Collision for 75-step SHA-1: Intensive Parallelization with GPU

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Abstract

We present a brief report on the collision search for the reduced SHA-1. With a few improvements to our previous work, directed at efficient parallelization on a GPU cluster, we managed to construct a new collision for 75-step reduced SHA-1 hash function.

1 Introduction

Recently we have constructed a new 2-block collision for 72-step SHA-1 and another one for 73-step SHA-1 in [1]. Our previous work has improved the method for the automatic construction suggested by Christophe De Canniére and Christian Rechberger in [2], [3].

In this report we focus on the intensive parallelization with GPUs. As our previous algorithm required large amount of computing power, extending it to GPUs seems natural. This results in some changes in the search of characteristics, and also in implementation. Using GPU, we were able to construct a new 2-block collision for 75-step SHA-1.

2 Improvements in the search of characteristics

We refer to [2] for the detailed description of basic method and notations and to [1] for our previous improvements, which are still used.

The search is naturally divided into *generating* part and *testing* part: on the first 16 steps many possible messages are generated and later every message is only tested and can be either accepted or rejected, but does not produce any new messages.

The algorithm is trivially parallelizable. Therefore, the main challenge to its performance on GPU is *coherency*, i.e. similarity of control flow between threads in a warp. We noticed during experiments that coherency can be improved, if the characteristic has many free bit positions in the last few steps of the generating part, and has very little freedoms in the 5 steps which immediately preceed the GPU part.

To take this effect into account, we modify the stage 2 of the method, namely random trials of positions where to impose the – restriction. Namely, we decrease the probability to select a position from the last steps of the generating part, so restrictions tend to concentrate on the first steps. This seems to increase the final workfactor slightly, but the gain from the higher coherency more than compensates this.

We also note that the automatic search of the characteristics can be improved with the following trick. First, we find some characteristics. Second, we look in the first few steps

of the testing part, examine the conditions which increase P_u , and copy these conditions to the initial characteristics. Next, we run the automatic search again, starting from the initial characteristics with new conditions. If the number of added conditions is not too large, then the automated search still has considerable freedom and can produce even better characteristics.

3 GPU Implementation

Generating part can be naturally viewed as backtracking search, and the testing part is built into the search as a check at the final round. Generating part can be subdivided into CPU part and GPU part. During CPU part, the tree is unfolded to a certain search depth, so that enough *search stacks* is generated to make use of GPU parallelism. The unfold depth is currently selected manually for each characteristic after initial experimentation. Too small a depth will result in insufficient parallelism, and thus underutilization of GPUs, while too large a depth will require too much GPU memory. During experiments we have found out that about 100,000 search stacks per GPU is required to utilize it efficiently.

During GPU part, all stacks are searched in parallel by multiple GPUs. If search is finished for a stack, that stack is removed; no new stacks are generated during GPU part. The main GPU kernel implements backtracking search and testing part. In this kernel, each thread works on a single search stack. For each invocation of the main kernel, each thread does a fixed number of search steps, and then finishes its work. Main kernel also collects statistical data, which include number of nodes traversed and maximum depth reached. Between kernel invocations, checks for maximum depth are performed, and an array of stacks is compacted if necessary.

Computations are distributed on a cluster using MPI. Each MPI process is assigned to a single GPU. Search stacks are distributed in block-cyclic fashion among processes. Each process generates all seach stacks, and discards those which do not belong to it. Initially, there was a global barrier after each invocation of main GPU kernel. However, experimental data has shown that this global barrier can increase runtime by a factor of 2 for certain characteristics. Therefore, in subsequent implementations, there is no global barrier. Instead, master process (which has rank 0) spawns a separate thread for collection of statistics, and other processes report statistical data to that thread after each invocation of the main GPU kernel. Process 0 also spawns another thread, which displays aggregate statistics at regular intervals, every minute by default.

We used NUDA (Nemerle Unified Device Architecture) [4], a set of GPGPU extensions for Nemerle, for implementation. It was chosen because it is open-source and provides a higher-level view of GPU programming. It also handles low-level details, such as data transfer and marshalling of parameters. Internally, NUDA uses OpenCL to generate code for loops sent to GPU.

In our initial implementation, back-tracking search was implemented as a single loop, with stages requiring special handling implemented as conditionals. There were 2 such stages: switching between search rounds, where additional values needed to be precomputed, and testing the generated message. Testing was implemented in a separate function, the loop along testing rounds being fully unrolled using NUDA's inline annotation.

However, while performance of our initial implementation was good for some characteristics, it was awful for other ones. Specifically, while 60% efficiency was reached on 73-1 characteristic, only 15% was attained on 72-2. Such low performance is due to low coherency between neighbouring threads. We applied two optimizations to increase coherency. The first optimization was sorting the search stacks after each main kernel invocation. We quickly established that using stable sort was better than unstable sort (e.g. quicksort), as it preserves the order of values with same keys, and thus preserves coherency. We also experimented with various sorting keys, but finally settled on using the value being searched at the current round. On 72-2, stable sorting searched value gave about 45% increase in performance compared to initial implementation. Stable sort was implemented on GPU using radix sorting algorithm [5], and experiments have shown that time spent in sorting stacks is negligible compared to time spent in backtracking search.

The second optimization was replacing the single-loop implementation of backtracking search with triple-loop nest implementation. The innermost loop only traverses nodes and checks for characteristics inside a single round, until either a good node is found, or all nodes of this round have been searched. The second innermost loop implements message testing at the final search round. This allows to check messages without incurring the overhead of round switching. As more that 75% of time is spent in message testing for some characteristics, this improves performance. Finally, the outermost loop performs switching between rounds, and also checks conditions for kernel termination. It was shown that triple-loop configuration is far better in preserving coherency than single-loop configuration. Together, triple-loop and stable sort by round value gave about 2x improvement over initial implementation for 75-1 characteristic.

A number of additional optimizations has been performed. This included using constant memory for storing characteristics, and using shared on-chip memory for storing search stacks. Contrary to our expectations, using shared memory gave only 2.5% improvement over using global memory. This indicates that the memory footprint of the algorithm fits well into L1 cache of NVidia Fermi GPUs, which were used for computations. We also modified the algorithm used for generation of characteristics, as described in the previous section, to provide better coherency. The final version used for 75-round collision search incorporated all optimizations described above.

Because the second run was estimated to take much longer time, support for checkpoints has been integrated into the application. And since the number of available GPUs was expected to fluctuate, checkpointing implementation also supported starting from a checkpoint with different number of processes than the checkpoint was originally generated with. As there is no global synchronization between processes during GPU part, each process writes the checkpoint independently to its file at fixed time intervals, by default once each hour.

4 Calculations

Initial experiments and tuning were performed on "GraphIT!" system installed at Research Computing Center, Lomonosov Moscow State University (RCC MSU). This system has 16 nodes, each equipped with 3 NVidia Fermi M2050 GPUs, each having 3 GB of GPU memory. This gives a total of 48 GPUs, however, no more that 30 of them were used for computational experiments.

Final computations were performed on GPU partition of "Lomonosov", currently the most powerful supercomputer in Russia, also installed at RCC MSU. Each GPU node of "Lomonosov" has 2 NVidia Fermi X2070 GPUs, each having 6 GB of GPU memory. As the system is still in beta stage, not all nodes are available for the end users.

For the first block, the estimated work factor was 2^{58} traversed nodes. Due to constraints on messages, the characteristic was split into 4 parts, and one of them was chosen for the initial run. The run was performed on 264 GPUs, and took 11000 seconds to find the first collision block. The actual number of nodes traversed was $2^{54.06}$. Here, we count both search rounds and testing rounds as nodes, though the latter takes about 2.5 more time to compute than the former. For the first block, about 40% were testing rounds, with the rest being search rounds.

The second block has an estimated work factor of $2^{63.01}$ traversed nodes. It started on 320 GPUs, and was restarted from checkpoints multiple times due to node failure or availability of additional GPUs. It finished with 512 GPUs. Based on logs, we estimate that 455 GPUs on average were used. The entire computation took 1904252 seconds, or 22 days and 45 minutes, and traversed a total of $2^{61.92}$ nodes of the search tree. About 58.8% of them were testing rounds, and the rest were search rounds. Computational efficiency during the second run was estimated at 52% (of peak GPU performance). Had the full partition with 1554 GPUs been operational, the entire computation would still require 6.5 days to complete.

In both cases, we had some "luck", as it took less time to find the collision block than it had been originally estimated. Specifically, computation finished about 16 times faster in the first case, and about 2 times faster in the second case. If not for this "luck", the entire computation would have taken 1.5 month to complete.

Comparing current GPU implementation with the previous parallel search implementation in [1], we estimate a single GPU to be as fast as 39 x86 CPU cores. Thus the equivalent number of CPU cores for the second computation would be 17745, which is about the same number used in our previous computation. However, given the demand for CPUs on "Lomonosov", it was highly unlikely that we could get so many cores for several weeks. The demand for GPUs was much lower, and it was therefore possible to get the required number of GPU cores for the required time.

5 Acknowledgements

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A Collision for the 75-step reduced SHA-1

Ta	ble 1.	Example of a	75-step SHA-1	collision using the standard I	[V]
	i	Message 1,	first block	Message 1, second block	

a	ble 1.	Examp	ole of a	75-step	SHA-1	collisio	n using	the sta	andard I	
[i	Message 1, first block				Message 1, second block				
	1-4	F01EE8EE	BDDFF313	B2F59EE4	BB37F2BB	F072633F	0D32226A	DFF74459	98507743	
	5 - 8	2F472A36	1C052F6A	96403EF0	F144298B	EEFE63DD	FE10D5C5	AFE33902	EF74984E	
	9-12	DAF5519C	7A90DD71	2BF3718E	A7E3DE6D	350272F7	DB382ABC	155B0414	B800179D	
l	13 - 16	EFFA975E	9B00AA95	6056E3EE	2BA4483A	18ECD4BC	15497213	1505284C	60C4F869	
[i		Message 2,	first block		l	Message 2, s	second block	ς	
ĺ	1-4	001EE884	3DDFF353	22F59E94	0B37F2E8	00726355	8D32222A	4FF74429	28507710	
	5 - 8	1F472A3E	1C052F29	46403E82	4144299B	DEFE63D5	FE10D586	7FE33970	5F74985E	
	9-12	2AF551FE	BA90DD33	2BF371BE	47E3DE2F	C5027295	1B382AFE	155B0424	580017DF	
	13 - 16	CFFA973E	7B00AAD4	4056E3BE	EBA4487B	38ECD4DC	F5497252	3505281C	A0C4F828	
[i			XOR-differ	ences are th	e same for b	oth blocks			
	1-4	F00006A	80000040	90000070	B0000053	F000006A	80000040	90000070	B0000053	
	5 - 8	3000008	0000043	D0000072	B0000010	3000008	0000043	D0000072	B0000010	
	9-12	F0000062	C0000042	0000030	E0000042	F0000062	C0000042	0000030	E0000042	
l	13 - 16	20000060	E0000041	20000050	C0000041	20000060	E0000041	20000050	C0000041	
[i	The colliding hash values								
[1 - 5	3DF7F21E	130079F3	C2E6EFFF	FD9C4141	9AA8723A				

B Characteristics for the 75-step reduced SHA-1

$ \begin{array}{cccccccccccccccccccccccccccccccccccc$		Table 2. Characteristics used for the first block of the 75-step collision							
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$ \begin{array}{cccccccccccccccccccccccccccccccccccc$			111000000010-0111101110	10	-0.28	0.00	0.00		
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$							0.06		
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$						0.00	9.87		
$ \begin{array}{c} 5: \\ 0.0106-0110011001100000-0-110100000 \\ 0.0001110001000-0-0011001 \\ 0.000 0.00 16. \\ 0.000-011010011100100-000000 \\ 0.000 0.00 0.00 \\ 0.00 0.00 $	3:		u0uu10001n1u10uu				15.54		
	4:	1un1uu011unu1u0-000-10-111110u10	00un11110011n110	2	-4.19	-4.19	18.54		
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$	5:	nnnn00uun011000nu00-0-1101uu0010		2	-2.34	-2.13	16.35		
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$		0100n0101n0111-1001u0-u000uuu011		2	0.00	0.00	16.01		
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	75:								

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-4:	$\frac{\nabla A_i}{01001110010010001100001n000}$	∇W_i	F_W	$P_u(i)$	$P_c(i)$	$N_s(i)$
-4.	1011011001010111111000100010001000110000					
-2:	000001100111001110110101010u10010					
-1:	010001110000111001101011101n1000					
0:	11100000000001001100101111110101	uuuu0000010110nu1u1u1	8	0.00	0.00	0.00
1:	000n10001010-10-10010n0nn0	n0001110100u101010	4	-0.42	-0.42	3.69
2:	n110111010110111-11n1n0010u00	u10u111111111-00unu1001	6	-0.96	-0.83	7.28
3: 4:	u0un1100010101-n-n-0-0uun1n1n1 101n0n0110nu1uu1-01u-uun011101nn	u0nu1000u0n00uu 11un1111101u101	$\begin{vmatrix} 2\\ 2 \end{vmatrix}$	$0.00 \\ 0.00$	$0.00 \\ 0.00$	12.31 14.31
5:	uuuuuuu1n0101u10uu1-1-n0u00u10n	1111111000011u0001nu		-2.00	-2.00	14.31 16.31
6:	10001000u1101n00-n-uu0-1110nn01n	un1n1111111nnn00u0		-1.00	-1.00	17.31
7:	n110101unn1000u0110110011011un	u1un111101110n1110	4	0.00	0.00	18.31
8:	0100001001001uu0000100001000	nnuu010100-uu101u1	3	-0.05	0.00	22.31
9:	0011100001000-0-n01-1u001n1n011n	uu011011n1111n0	8	-0.02	0.00	25.27
10:	n01000001011-u1uuu01nn1u1 1011100001110101n0100n00n1uu0n	000101010nu0100 unu11000000000011n0111n1	1	-1.10	-1.09	33.24
$11: \\ 12: $	11001011111111111-0111001001	00n11001nu11100	5 9	$-3.64 \\ 0.00$	-2.98 0.00	$33.15 \\ 34.50$
12.13:	10010010001000-011111n01	nnn1010n01001u	6	0.00	0.00	43.50
14:	n1001011111111-0-0101000	00n1011u0n1100	9	-7.22	0.00	49.50
15:	111101-101111u-1001101	nu1000-01u10100u	10	-0.21	0.00	51.29
16:	n-0010-11000n01	nnn11110nnn01n0	0	-0.07	-0.03	61.07
17:	0-111nu0	u0u1011101100un		-3.00	-2.68	61.00
18:	n-0-00 00	un0010111u00u0		-1.00	-0.83	58.00
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$\frac{20.}{21:}$	<u>II</u>	00n1110101010u		-1.00	-1.00	56.00
$\frac{211}{22:}$		nn01100000011n0	0 0	-2.00	-2.00	55.00
23:	n-	nnn1010u1100n1	Ŏ	-2.00	-2.00	53.00
24:	n-	0un0-00u1001n0	0	-1.00	-1.00	51.00
25:		u00110001111u1		-1.00	-1.00	50.00
26:		00100-001010111		0.00		49.00
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31:		1010011100100	0	-2.00	-2.00	48.00
32:	n-	u00-0101u000100	0	0.00	-0.00	46.00
33:		n-1-11011011110		-2.00	-2.00	46.00
34:	n-	101011u000101 u0-0010000100u		0.00	0.00	44.00
35: 36:	n	-1-110000100u		$-2.00 \\ 0.00$	-2.00 0.00	$ \begin{array}{c} 44.00 \\ 42.00 \end{array} $
37:		n111001000un	0 0	-1.00	-1.00	42.00
38:		1x010111110n0	ŏ	-2.00	-1.00	41.00
39:	n-	ux1011u11000-	0	-1.00	0.00	39.00
40:		nn01101010u1	0	-1.00	-1.00	38.00
41:		x10-0001100111		-1.00	-1.00	37.00
42:		x111011101-1 u01111100n1		-1.00	-1.00	36.00
43: 44:	n-	0000u10000-		$-1.00 \\ 0.00$	-1.00 -0.00	$35.00 \\ 34.00$
45:		01010000-u-	l ő	-1.00	-1.00	34.00
46:		x11100100000	ŏ	-1.00	-1.00	33.00
47:		n-0-11010101-0	0	-1.00	-1.00	32.00
48:		x-1000101-0-0	0	0.00	-0.00	31.00
49:		001001000n-		-1.00	-0.42	31.00
50:	n-	1010u101-0- -011000-0-0-		0.00	-0.00	30.00
51: 52:	n	x11101u0101		-2.00 -1.00	-1.42 -1.00	$ \begin{array}{c} 30.00 \\ 28.00 \end{array} $
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54:		00111-0-1		-1.00	-1.00	25.00
55:		x00000101	ŏ	-1.00	-1.00	24.00
56:		x101111-1	0	0.00	0.00	23.00
57:		101-1-01		0.00	-0.00	23.00
58:		10010100		0.00	-0.00	23.00
59: 60:		0-01100-10-0-		$\begin{array}{c} 0.00 \\ 0.00 \end{array}$	$ \begin{array}{c c} 0.00 \\ 0.00 \end{array} $	$23.00 \\ 23.00$
61:		100000		0.00	-0.00	23.00 23.00
62:		-1110-0	0 0	0.00	0.00	23.00
63:		0-0-1n	Ŏ	-1.00	-0.19	23.00
64:	n	1-101u001-	0	0.00	0.00	22.00
65:		111-01-0x		-1.00	0.00	22.00
66: 67:		1-0-1nx		-2.00	-0.19	21.00
$\begin{array}{c c} 67: \\ 68: \end{array}$	n n	111u1n-x 110-uxu		-2.00 -1.00	-0.42 -0.00	$19.00 \\ 17.00$
69:	n			-3.00	-0.36	16.00
70:	u	0n10u-xx	0 0	-3.00	-0.42	13.00
71:	u	1-n0-1xn-ux	ŏ	-3.00	-0.42	10.00
72:	n	0-un-xx-u	0	-3.00	-0.36	7.00
73:	n	u1uxxx-		-4.00	-0.91	4.00
74:	uu	nxn	0	-1.00	-0.00	1.00
75:						