Dora: Processor Expressiveness is (Nearly) Free in Zero-Knowledge for RAM Programs

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Abstract

Existing protocols for proving the correct execution of a RAM program in zero-knowledge are plagued by a *processor expressiveness tradeoff*: supporting fewer instructions results in smaller processor circuits (which improves performance), but may result in more program execution steps because non-supported instruction must be emulated over multiple processor steps (which diminishes performance).

We present Dora, a concretely efficient zero-knowledge protocol for RAM programs that sidesteps this tension by making it (nearly) free to add additional instructions to the processor. The computational and communication complexity of proving each step of a computation in Dora, is *constant* in the number of supported instructions. Dora is also highly generic and only assumes the existence of linearly homomorphic commitments. We implement Dora and demonstrate that on commodity hardware it can prove the correct execution of a processor with thousands of instruction, each of which has thousands of gates, in just a few milliseconds per step.

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Contents

1 Introduction

Zero-knowledge proofs and arguments [GMR85, GMW86] empower a prover to convince the verifier that some public statement x is a member of an NP language $\mathcal{L}$ without revealing anything beyond membership itself. A long line of work has demonstrated feasibility of practically efficient zero-knowledge systems [GS08, JKO13, GGPR13, BCC+16, Gro16, KKW18, BBB+18, BCR+19, GWC19, Set20, HK20b, BMRS21, WYKW21, YSWW21, WYX+21, WYY+22, BBMHS22, YHKD22]. As a result, zero-knowledge proofs are now being regularly integrated as a key component of deployed systems [BCG+14, Zav20, se19]. However, most concretely efficient and deployed zero-knowledge proof systems are *circuit zero-knowledge*, *i.e.,* they work with a circuit representation of the NP relation.

Zero-knowledge for RAM Programs. For many applications of zero-knowledge, *RAM zero-knowledge*—i.e., proving the correct execution of a public RAM program on some secret inputs—might be desirable. For instance, RAM program representation of relations may be more efficient than circuit representations (e.g., sorting) or the RAM program itself might be of special interest (e.g., the prover might want to demonstrate knowledge of a software exploit against the RAM program [HK20b, GHAH+23]). One straight-forward approach to RAM zero-knowledge, eg. [HK20b], is to use a circuit compiler to transform a source code representation of a RAM program directly into a circuit capturing the same functionality, and then feed the resulting circuit to the prover of an existing circuit zero-knowledge system. This approach, however, introduces several inefficiencies: the resulting circuit must be input-independent, all loops must be unrolled for a fixed number of iterations, and all input-dependent conditional branches are part of the circuit description[1].

Instead, the state-of-the-art approach to RAM zero-knowledge [BCG+13, BCG+13, BCTV14b, BCTV14a, HK20a, HYDK21, HK21, FKL+21, dOTV22] relies on modeling a processor and memory access as circuits. To demonstrate that a step of the computation was executed correctly, the prover uses circuit zero-knowledge to prove that the new program state is an outcome of a *valid state transition* from the previous program state, where the transitions functions are determined by the processor's instructions.

The Expressiveness Tradeoff. Designing an optimized processor circuit to use within RAM zero-knowledge requires grappling with an *expressiveness tradeoff*. It is natural to want a very *small* processor circuit with very few instructions, as the prover must "pay" for all the instructions in the processor in each step of the proof—even unused instructions. Indeed, minimizing processor size in this way has become standard practice; Ben-Sasson et al. [BCG+13, BCTV14b] introduced a processor called TinyRAM with only 29 instructions for this purpose, and recent works have created other processors with even fewer instructions [HK20a, HYDK21, FKL+21]. This approach, however, results in *more* steps of program execution—potentially negating the value of a smaller circuit—because instructions not included in the processor must be *emulated* over multiple processor steps. Finding the right balance between processor expressiveness (i.e., how many instructions it supports) and program length is a highly nuanced engineering problem and will depend on the specific RAM program being considered.

In this work, we propose a new approach to RAM zero-knowledge that avoids the expressiveness tradeoff altogether. Our work leverages the observation that the processor circuit has a very specific structure; namely, that it is a *disjunction* of the supported instructions. A sequence of recent works on disjunctive zero-knowledge [HK20b, BMRS21, GGHAK22b, KST22, KS22, GHAKS22, KS23] have shown that it is possible to design zero-knowledge protocols with prover complexity proportional only to the size of the largest clause in the disjunction. Within the context of RAM zero-knowledge, this would allow adding additional instructions to the processor circuit for free, thereby increasing expressiveness. Although some of these works have studied applying these techniques to RAM computations within the context of incrementally verifiable computation [KS22], adapting this intuition to achieve *concretely efficient* RAM zero-knowledge remains an open question.

1.1 Our Contributions

In our work, we present Dora, a concretely efficient zero-knowledge proof system for RAM programs. Dora provides a new way out of the *expressiveness tradeoff*, by supporting increased processor expressiveness for free (both in terms of computation and communication). Concretely, Dora has the following desirable attributes:

[1] As discussed below, some recent work has shown how to avoid the communication costs associated with branching.

- *Communication Complexity:* The communication complexity of Dora is $O(t + \ell)$, where t is the number of steps of the computation and ℓ is the number of instructions supported by the processor. Notably, the prover and verifier exchange a constant number elements to prove the correct execution of a step of the computation, no matter the number of instructions supported by the processor. Dora is the first protocol to have this asymptotic behavior.
- *Computation Complexity:* The computation complexity of Dora is also $O(t + \ell)$. Concretely, the verifier sends just a single field element in each step of the computation and the prover's per-step computation depends only on the size of the instruction being executed in that step. Dora is the first protocol to have this asymptotic behavior.
- *Generic Approach and Fiat-Shamir Friendly:* Our approach carefully combines new techniques with insights from recent work on disjunctive zero-knowledge [HK20b, GGHAK22b, GHAKS22] and incrementally verifiable computation [KST22, KS22]. Dora only assumes the existence of a linearly homomorphic commitment scheme, the optimal choice for which can be selected based on the deployment considerations. For example, if Dora was deployed in an interactive setting, VOLE-based techniques [BCGI18, YWL+20, BMRS21, YSWW21, WYKW21, BBMH+21] can be used, whereas Pedersen commitments [Ped92] can be substituted when non-interactivity is desirable. If the commitment scheme is post-quantum secure, then Dora will also be post-quantum secure. Finally, the verifier in Dora is public coin, making it Fiat-Shamir friendly [FS87].
- *Concretely Efficient:* The techniques introduced in Dora are concretely efficient. We implement Dora and integrate it into the `swanky` [Gal19] framework. The marginal cost of proving an additional step of computation with Dora is on the order of milliseconds. For example, if each instruction has 2^9 gates, then Dora, when run on commodity hardware, can prove correct execution of a program at $>$400 steps per second—no matter how expressive the processor instruction set.

To construct Dora, we introduce a new building block for construction zero-knowledge primitives called the *zero-knowledge bag* (or ZKBag), which is the heart of our approach to both proving execution of the processor circuit and ensuring that the prover accesses memory honestly. ZKBag is a construct that allows values to be inserted and removed, and ensures that (1) a prover can only remove values inserted in the ZKBag and that have not previously been removed, and (2) a verifier cannot learn a correspondence between an item inserted into the ZKBag and the removed value. This ZKBag primitive may be valuable—both conceptually and concretely—in constructing other protocols.

1.2 Related Work

Zero-knowledge for RAM programs emerged as a practical problem of interest following the work of Ben-Sasson et al. [BCGT13, BCG+13, BCTV14b, BCTV14a], which demonstrated that it was feasible to prove the correct execution of real RAM programs. As discussed more in Section 2.1, these works laid out the primary template from which we work. Recent works have demonstrated how to get better concrete performance, including the work of Heath et al. [HK20a, HYDK21, HK21], Franzese et al. [FKL+21] and Delpech de Saint Guilhem et al. [dOTV22]. These works have demonstrated concrete efficiency, but still must pay the cost of the full processor circuit in each step. Another common approach to proving correct execution of RAM programs is to "unroll" the program into an explicit circuit which can be prover with generic zero-knowledge techniques, eg. [CK18, YSWW21, WYKW21]. The demonstration that these approaches are efficient and scalable has led to studying new applications of zero-knowledge for RAM programs, eg. proofs that a program can be exploited [HK20b, GHAH+23, CHP+23].

In reducing the computation and communication complexity of executing one step of the processor to be independent of the number of instructions, we leverage the disjunctive structure of processors. Zero-knowledge that is optimized for disjunctions has been the focus of foundational work on zero-knowledge [CDS94, AOS02, GMY03] and a significant number of recent work [GK15, CPS+16, Kol18, HK20b, GGHAK22b, ACF21, BMRS21, GHAKS22]. Generally, these works exploit the observation that the *prover* knows which clause of the disjunction is satisfied, and therefore the work on the remaining clauses is "wasted." This means that protocols can be designed, eg. [HK20b, GGHAK22b, ACF21, BMRS21], that have communication complexity the depends mostly on the size of the largest clause in the disjunctions (possibly with logarithmic overhead). Our work can be seen as developing specialized disjunctive zero-knowledge techniques that compose well with RAM access and have efficient computation time.

Incrementally Verifiable Computation. Our works builds on two recent results on building incrementally verifiable computation (IVC) from folding schemes, Nova [KST22] and SuperNova [KS22], which are a part of an emerging literature on concretely efficient IVC [BGH19, BCMS20, BDFG21, BCL+21]. In Nova [KST22] , Kothapalli et al. show how to build a folding scheme for NP using a generalization of R1CS called *Relaxed R1CS* and show how it can be used to build IVC. Kothapalli and Setty then proposed SuperNova [KS22], an extension of Nova that supports *non-uniform* IVC for "free," and discuss how to apply their techniques to verifying processor computations.

Zero-knowledge proofs for RAM program execution can be seen as a version of non-uniform IVC where the prover must also hide *which* instructions are applied to the state at each step of the computation, but also need not be fully succinct in the number of steps. Zero-knowledge is not a goal of SuperNova, and thus we require new techniques to leverage their approach into our setting. Additionally, SuperNova's IVC reasons over the entire contents of memory, which is not concretely efficient; instead, we couple our zero-knowledge IVC with a separate protocol for managing memory consistency. Kothapalli and Setty have also recently introduced HyperNova [KS23], which aims to develop new folding schemes for NP that can be used to build more efficient IVC.

Other SNARKs. There are other prior works [WSR+15, ZGK+18, KPPS20, BBHR18, lib18, gen20, hod21, GPR21, MAGABMMT23, DXNT23, CGG+23] that focus on building concretely efficient zkSNARKs (zero-knowledge succinct non-interactive arguments of knowledge), where the prover cost grows only with the size of the program execution. For instance, Buffet [WSR+15], vRAM [ZGK+18], Mirage [KPPS20], MUX-Marlin [DXNT23] and Sublonk [CGG+23] that consider an "a la carte" cost profile for the provers where the prover cost for proving a step of computation grow only with the size of the circuit representing the instruction invoked on that step, i.e. independent of the number of branches. However, these schemes require a trusted common reference string setup and make use of expensive public-key operations. Works building on zkSTARKs [BBHR18, lib18, gen20, hod21, GPR21, MAGABMMT23] use a transparent (i.e. untrusted) setup and require the prover to only do work proportional to the execution trace. However, they require making a non-black box use of cryptographic hash functions. Similarly, commit and prove style SNARKs that [CFQ19, Lip16, CFH+15] that have similar prover computation times also make non-black box use of cryptographic commitments. Therefore, while all of these schemes have sublinear proof sizes, their prover computation times are significantly worse than those resulting from known techniques for zero-knowledge with non-sublinear sized proofs.

Concurrent Work. Two works, developed concurrently with our own, take aim at more efficient zero-knowledge random access memory [YH23] and proving statements with processor-like structures [YHH+23]. Our works provide different methods that arrive at similar concrete results. We include a best-effort comparison to these concurrent works in Appendix A.

2 Technical Overview

We now give an overview of the key techniques we use to construct Dora. We first recall the basic template to achieving zero-knowledge for RAM programs before proceeding to Dora itself.

2.1 Background: Template for RAM Zero-knowledge

As discussed earlier, while zero-knowledge has primarily been studied in the circuit model (i.e., where the relation for the NP language is represented as a circuit over a finite field), a significant line of work has studied how to achieve zero-knowledge for RAM programs [BCGT13, BCG+13, BCTV14b, HK20a, HYDK21, GHAH+23]. The key idea in these works is to bootstrap from circuit zero-knowledge to RAM zero-knowledge by representing the RAM machine on which the program should be evaluated as an explicit circuit. The prover can then use this circuit as a state transition function, and show (in zero-knowledge) that repeatedly applying this circuit t times to some initial inputs, results in a desired final processor state.

More concretely, the prover and verifier represent the RAM machine using two components: (1) a *processor circuit* C_{proc}, and (2) a *memory checker circuit* C_{mem}. C_{proc} takes as input, values fetched from memory and implements a set of valid instructions $\mathcal{I} = \{I_1, \ldots, I_\ell\}$, one of which is evaluated over the inputs. For example, the I_i might add

values, test values for equality, or modify the processor state to affect control flow etc. The result of this evaluation can then be stored back in memory.[2] The memory checker circuit C_{mem} enforces that memory is treated consistently – that is, when a value is read from a particular memory address, C_{mem} checks to make sure that the value corresponds exactly to the last value written to that memory address.

Because most approaches to instantiating zero-knowledge for RAM program relies on this bootstrapping approach, the key determinant of efficiency is the *size* of the circuits required to implement the functionality C_{proc} and C_{mem}.

- **Current Approaches to C_{proc}.** Prior work has emphasized the need for a *small* C_{proc}, at the expense of expressiveness. For example, Ben-Sasson et al. [BCG+13] describe a minimal C_{proc} called TinyRAM, which contains 27 instruction that can be represented in ≤ 972 gates.[3] This is because the final circuit contains t copies of C_{proc}, and t can be very large. Thus, if a particular instruction I_i is very rarely used (in an average program), the prover and verifier still *pay* for that instruction in each step of the program execution. It may be more efficient to instead *emulate* I_i using a sequential series of other instructions, increasing the value of t. In practice, this emulation approach is concretely efficient – executing a RAM program on a TinyRAM only increases t by a multiplicative factor of 2-6x compared to x86, which contains hundreds of instructions.
- **Current Approaches to C_{mem}.** There are two primary approaches to checking the consistency of memory accesses discussed in prior works: (1) leverage an efficient oblivious RAM (ORAM) construction, or (2) use a *permutation proof*. In the former approach, the prover stores tuples of the form $(\textsc{address}, \textsc{value})$ within an ORAM (eg. [MRS17]), which is either maintained by the verifier (if the proof will be executed interactively) or represented in a non-black box manner within C_{mem}. Since ORAM constructions hide access patterns and can guarantee consistency, the verifier can be confident that memory has been treated honestly without learning anything about the program execution. The other approach has the prover generate a *memory trace* of all reads and writes during program execution. The prover then permutes this trace to be sorted by address (tie-broken by timestamp), and C_{mem} needs to only check that neighboring elements of the sorted trace are internally consistent. This later approach has been found to be more efficient in practice, and is thus the primary approach used in prior work focused on concrete efficiency [FKL+21, dOTV22, GHAH+23].

2.2 Zero-Knowledge Bag

The natural *physical analogy* of the zero-knowledge bag (ZKBag) is an opaque bag filled with identical envelopes: imagine the prover has an *physical bag* made of opaque material. Into this bag they can insert letters contained inside identical envelopes. Later, the prover can reach into the bag and remove one of the envelopes. Because the bag's material is opaque and all of the objects are wrapped in identical-looking envelopes, an observer cannot tell when the wrapped letter was put into the bag, and which one has been retrieved. However, no letter can be retrieved if it was not previously inserted. To make these properties more explicit, a ZKBag provides the following (informal) guarantees:

1. *Unique Removal*: Once an element has been retrieved from the ZKBag, it cannot be retrieved again (unless, of course, it is re-inserted).
2. *Ordered Binding*: Every element that is retrieved from the bag is exactly one of the elements that was previously inserted into the ZKBag.
3. *Order Hiding*: The act of retrieving an element from the ZKBag reveals nothing about when that element was inserted.

Clearly, in order to realize the *order hiding* property, elements cannot be inserted into the ZKBag in the clear, or else a verifier could trivially link insertions and retrievals based on the value itself. Instead, we have the prover wrap the elements using *commitments* when inserting into ZKBag; when the verifier wants to remove a value, it creates a

[2] Hardware architectures also have local memory, i.e., registers and program counter, within the processor circuit. For the purposes of this overview, we elide these low level details, but note that they can either be handled as *state* within the processor circuit or simply as a specially named memory region.

[3] For simplicity, we do not yet make a distinction between the number of gates needed to *compute* the instructions and the number of gates needed to *verify* that a claimed evaluation is correct. In practice, we always mean the latter.

new, fresh commitment to the value and convinces the verifier that the value therein corresponds to a value currently within the bag. This process should also remove the commitment from the bag, so that it cannot be retrieved again.

Looking ahead, ZKBag provides the right combination between binding and pattern hiding required to construct zero-knowledge for RAM programs. The relationship between ZKBag and memory consistency should be clear: writing to memory corresponds exactly to inserting a (ADDRESS, VALUE) tuple into a ZKBag, and reading from memory corresponds exactly to retrieving a (ADDRESS, VALUE) tuple from a ZKBag. We will also use a ZKBag to hold the instruction set $\mathcal{I}$ for the processor, and have the prover pick out one instruction to be evaluated in each processor step (before reinserting it).

Constructing a ZKBag. It is clear to see that ZKBag is closely reminiscent of many existing cryptographic primitives.

If *unique removal* were not required, ZKBag could be realized directly with *set membership proofs*, a concretely efficient primitive that has been the subject of immense recent study (eg. [RST01, CCs08, BCF+21, GGHAK22a, CGT23]). To achieve *unique removal*, it is clear that some kind of oblivious revocation is required, a technique that has been used in multiple other contexts, eg. ZCash [MGGR13]. However, a set membership based approach will require that the statement for each retrieval *grows* as the protocol continues.[4] Ideally, we want each insertion and retrieval to require a *constant* amount of communication and computation, as these interfaces will be called many (ie. $\mathcal{O}(t)$) times.

To achieve constant overhead, we batch the checks required for *ordered binding* and *unique removal* across all insertions and retrievals, deferring the verification until the end of the protocol. In more detail, the prover and verifier maintain two lists of commitments: a list of insertions $\mathcal{I}$ and a list of retrievals $\mathcal{R}$. Each time the prover wants to insert a value v_i into the ZKBag, the verifier provides a uniformly random *tag* tag_i to the prover. The prover forms a *hiding commitment* $\mathsf{com}_{\mathsf{v}_i}$ to v_i: $\mathsf{com}_{\mathsf{v}_i} = \mathsf{Com}(v_i)$ and the parties jointly form a *public/non-hiding commitment* $\mathsf{com}_{\mathsf{tag}_i}$ to tag_i: $\mathsf{com}_{\mathsf{tag}_i} = \mathsf{Com}(\mathsf{tag}_i)$ with shared randomness. Both parties add $(\mathsf{com}_{\mathsf{tag}_i}, \mathsf{com}_{\mathsf{v}_i})$ to their respective insertion list $\mathcal{I}$. When retrieving a value v_j from the ZKBag, the prover recalls the tag tag_j generated during insertion, creates the *hiding* commitment tuple $(\mathsf{com}_{\mathsf{tag}_j} = \mathsf{Com}(\mathsf{tag}_j), \mathsf{com}_{\mathsf{v}_j} = \mathsf{Com}(v_j))$ using fresh randomness and both parties add $(\mathsf{com}_{\mathsf{tag}_j}, \mathsf{com}_{\mathsf{v}_j})$ to the their retrieval list $\mathcal{R}$.

When the protocol ends, the prover retrieves any remaining values from the bag (i.e., it empties the bag) and gives a permutation proof demonstrating that there exists a permutation ϕ such that $\mathcal{I} = \phi(\mathcal{R})$. It is easy to see that *Read-only access* to the ZKBag can be accomplished by removing a tuple $(\mathsf{com}_{\mathsf{tag}}, \mathsf{com}_{\mathsf{v}})$ from the bag and immediately re-inserting the same (non-rerandomized) value commitment with a freshly generated tag (ie. the tuple $(\mathsf{com}'_{\mathsf{tag}}, \mathsf{com}_{\mathsf{v}})$).

Intuitively, the use of hiding commitments provides the necessary *order hiding* property, and the tags provides both the *ordered binding* and *unique removal* properties. Specifically, a prover who wanted to remove an item that has not yet been inserted would need to predict the tag that the verifier would generate for that value in the future. Similarly, if an adversary removes the same value from the ZKBag twice, it must produce a *second* valid tag corresponding to the value. If the prover re-uses the same tag twice, there will be a mismatch in the tags in $\mathcal{I}$ and $\mathcal{R}$, and if it uses a new tag, it must predict a tag the verifier will generate in the future.

This construction is highly efficient. Each insertion and removal requires preparing and sending only two commitments. The batched check can be done with constant communication and linear computation using a Neff-style commit-and-prove style permutation proof [Nef01] (which we describe in Section 3.5).

2.3 Constructing Dora using ZKBag

In our work, we approach the problem of constructing efficient zero-knowledge for RAM programs at the *protocol* level, rather than trying to optimize the choice of circuits C_{proc} and C_{mem}.

Expressiveness Comes Free in Zero-Knowledge. The result is Dora, a protocol for RAM zero-knowledge that transcends the seemingly inherent tradeoff between processor expressiveness (i.e. $|\mathcal{I}|$) and execution trace length (i.e.

[4] We note that there is a recent line of work showing the set membership—and disjunctive zero-knowledge more generally—can be achieved with very low overhead as the statement size grows. While it may be possible to construct ZKBag from these primitives, we instead pursue another approach discussed below.

t) altogether, and instead shows that processor expressiveness can come (nearly) *free*[5]—both in terms of computation and communication.

As with prior attempts, Dora can be decomposed into a memory component and a processor instruction handling component, each of which we realize with ZKBag. Before describing the techniques that we use in Dora, we briefly recall our efficiency goals for each component:

- *Efficiency Goals for Memory Component:* During each step of execution, the prover will fetch (1) the value stored at the address indicated by the program counter, and (2) fetch a single value from memory and write a single value to memory, as either (or both) might be necessary for the next instruction. We require that the computation and communication complexity of each fetch and write must be *constant*.
- *Efficiency Goals for Processor Instruction Component:* During each step of execution, the prover will evaluate a *single* instruction on the processor state, where the instruction is determined by the value fetched in (1) above. We require that the communication and computation complexity of each step of execution is *independent* of the number of instructions in the instruction set $\mathcal{I}$.

We now discuss how to achieve both of our goals using ZKBag.

Handling Memory in Dora using ZKBag. As noted above, handling memory access with ZKBag is straightforward, as ZKBag's properties are virtually identical to those required for memory consistency. The prover and the verifier begin by initializing the memory space by inserting public tuples $(\textsc{address}, \textsc{value})$ into ZKBag for *every address* in the memory space, including the program code and the rest of the initial memory state (e.g. the initial stack and heap) of the execution.

When proving a step of the computation, the prover interacts with the memory store three times[6]:

(1) The prover begins by reading the next instruction from memory and loading it into the processor state. This is a read-only operation, which the prover achieves by removing and re-inserting the same value (i.e. the same commitment).

(2) The prover also reads a value from memory into the processor state in case the instruction that will be run in the next instruction needs to read memory (e.g. for a LOAD instruction). Just as above, this read is read-only. Note that the prover must always perform this read in every step of the computation in order to hide any witness-dependent read patterns.

(3) Finally, the prover performs an update to one address in memory in case the instruction run in that step is a STORE instruction. This write instruction requires removing an element from the ZKBag and then rewriting to the same address with a new value from the processor state.[7] If the instruction does not require performing a write instruction, the prover can simply rewrite the initial value leaving memory functionally unchanged.

Soundness follows directly from the *unique removal* and *ordered binding* properties of the ZKBag (discussed above), as these properties guarantee that the verifier knows that each values read from memory must be "current." Zero-knowledge relies on the *order hiding* property to hide the memory addresses being manipulated.

Using this protocol, the total complexity of managing memory in Dora is only three tuple insertions and three tuple removals per step of the computation, but this can be reduced because the prover does not need to resend the same commitments multiple times.

Handling Processor Instructions in Dora using ZKBag. During each step of processor execution, the prover needs to convince the verifier that a processor state st_{i+1} is the result of applying *one* of the instructions in the instruction set to the previous processor state st_i, without revealing which instruction was applied. We begin by giving a baseline approach for achieving our goal before proceeding to optimize the approach to improve concrete performance.

[5] In particular, we do not need to pay the cost of processor expressiveness at each step of the processor execution.

[6] We assume that the processor here has a simple load store architecture and all instructions in the instruction set read and write at most a single value. In more complex architectures (eg. architectures that support indirect loads) additional interactions with memory may be necessary. Extending the protocol to support such instructions is trivial.

[7] Ensuring that the read and write are to the same memory location can be easily ensured by reusing the address commitment retrieved during the removal.

Baseline Approach. A straightforward approach would be to use a *set membership* proof; the prover could generate a commitment to the executed instruction and then provide a proof that the contents of the commitment are a valid instruction. This commitment can then be added to the statement for another zero-knowledge proof that demonstrates the transition from st_i to st_{i+1}. This approach, while intuitive, has two primary downfalls:

(1) While there has been a tremendous amount of work on set membership proofs, state-of-the-art protocols have a *logarithmic* size in the number of elements in the set and a *linear* computation complexity in the size of the set [GGHAK22a, GGHAK22b]. While in practice it might be acceptable to tolerate the communication overhead, linear computation complexity may be unreasonable for large instruction sets. Moreover, our aim in this work is to achieve *constant* overhead—both in terms of communication and computation. While SNARKs might be a way to achieve our goals for the verifier, given SNARK's succinctness and constant-time verification, there is not an obvious way to use this set membership approach to get constant overhead for the prover.

(2) Given a commitment to the step's instruction I, the prover must then prove that st_{i+1} is the result of applying I to st_i. Doing this efficiently is non-trivial, given that the statement of interest is in committed form. A very natural approach to would be to combine non-black box use of the commitment scheme and universal circuits (ie. prove that I is in the commitment and that $U(I, \mathsf{st}_i) = \mathsf{st}_{i+1}$, where U is a universal circuit of the appropriate size), and then prove the resulting statement using generic, circuit zero-knowledge. Unfortunately, both non-black box use of cryptography and universal circuits tend to be highly inefficient, making this approach unattractive. It might be possible to design very specific zero-knowledge proofs that naturally interoperate the chosen commitment scheme to avoid the non-black box use of cryptography, but this approach would reduce the flexibility and modularity of our construction.

As such, the seemingly natural approach to handling processor instruction in Dora appears to be unfruitful. Instead, we investigate how ZKBag could be used to design a more efficient approach. As already demonstrated with memory management, ZKBag provides a highly efficient (ie. constant overhead) way to obliviously select elements from a set. As such, it seems natural to substitute the set-membership proof in the above template with ZKBag, resolving problem (1). However, using ZKBag in this way does nothing to resolve problem (2). As such, we require a slightly more nuanced approach to using ZKBag in order to achieve our result.

Combining ZKBag and Relaxed R1CS to Achieve Constant Overhead. Rather than store instructions in a ZKBag, we build on an approach from prior works on IVCs [KST22, KS22] and store a set of *accumulators* in the ZKBag—one accumulator for each instruction in the instruction set. Executing a step of the processor involves obliviously retrieving the appropriate accumulator from the ZKBag and updating it. The intuition behind this approach is to use these accumulators to iteratively update NP statements at each step, such that the prover can simultaneously verify the final accumulated set of $|\mathcal{I}|$ statements at the end of the protocol. These accumulators are carefully designed such that the prover's knowledge of a valid witness at the end of the protocol for each accumulated statement demonstrates that *each* step was correctly executed. The benefit of this approach is that the computationally expensive zero-knowledge proofs can be deferred until the end of the protocol, requiring only a single zero-knowledge proof for each instruction rather than for each step. This further improves the concrete complexity of Dora.

To instantiate these accumulators, we leverage *Relaxed R1CS folding*, an approach described by [KST22]. Relaxed R1CS is a natural extension to standard R1CS such that there can be additional error terms. A typical R1CS relation is constructed by matrices $\mathbf{A}, \mathbf{B}, \mathbf{C}$ and an instance $\vec{\mathsf{x}}$ is satisfied if there exists a witness $\vec{\mathsf{w}}$ such that $\mathbf{A} \cdot \vec{\mathsf{z}} \circ \mathbf{B} \cdot \vec{\mathsf{z}} = \mathbf{C} \cdot \vec{\mathsf{z}}$, where $\vec{\mathsf{z}} = \vec{\mathsf{w}} \| \vec{\mathsf{x}}$. A relaxed R1CS relation injects two additional *error* parameters, $\mathsf{u} \in \mathbb{F}$ and $\vec{\mathsf{e}} \in \mathbb{F}^m$, and is satisfied if there exists a $\vec{\mathsf{z}} = \vec{\mathsf{x}} \| \vec{\mathsf{w}} \| \mathsf{u}$ such that $(\mathbf{A} \cdot \vec{\mathsf{z}}) \circ (\mathbf{B} \cdot \vec{\mathsf{z}}) = \mathsf{u} \cdot (\mathbf{C} \cdot \vec{\mathsf{z}}) + \vec{\mathsf{e}}$. The power of relaxed R1CS is that it permits *folding*: given a fixed relation $\mathbf{A}, \mathbf{B}, \mathbf{C}$, and two instances $(\vec{\mathsf{x}}_1, \mathsf{u}_1, \vec{\mathsf{e}}_1)$ and $(\vec{\mathsf{x}}_2, \mathsf{u}_2, \vec{\mathsf{e}}_2)$, it is possible to combine the two into a new instance $(\vec{\mathsf{x}}, \mathsf{u}, \vec{\mathsf{e}})$ for the same relation $\mathbf{A}, \mathbf{B}, \mathbf{C}$. Importantly, a prover can only satisfy the new instance $(\vec{\mathsf{x}}, \mathsf{u}, \vec{\mathsf{e}})$ if they had valid witnesses $\vec{\mathsf{w}}_1, \vec{\mathsf{w}}_2$ to the initial instances (except with negligible probability). We defer the details of this folding procedure to Section 3.3.

Dora leverages this R1CS folding technique as follows: the prover and verifier initialize a ZKBag and (publicly) insert a relaxed R1CS instance (as defined by $\vec{\mathsf{e}}$ and $\vec{\mathsf{z}}$) for each instruction into the ZKBag that will be used as an accumulator. During each step of the computation, the prover retrieves the instance corresponding to the instruction that will be executed and prepares a new instance for the current instruction using the committed processor state and the values retrieved from memory. The prover then folds the state of the accumulator with the newly prepared

instance, locally updating the witness required to satisfy the combined instance. The prover then inserts the combined instance back into the ZKBag and is ready to continue to the next step. Once all the steps have been run, the prover removes the instance for each instruction from the ZKBag and opens them to the verifier. The prover and verifier then engage in a generic zero-knowledge proof for the final relaxed R1CS instances, allowing the prover to demonstrate that they have a witness that satisfies each. We note that there are several low-level details we have omitted in this description for clarity (e.g., the final instances must be randomized to satisfy zero-knowledge).

Putting It All Together. Dora is realized by combining the techniques described above for memory management and proving the correctness of instruction executions. In each step, the prover retrieves the appropriate values from memory and adds them to the (committed) processor state. The prover then uses the processor state to construct a relaxed R1CS instance that would prove correct execution of the instruction and folds it into the accumulator for the instruction executed in that step. Finally, the prover updates a memory location to emulate a store instruction. Once all of the steps have been completed, the prover opens all the accumulators and proves that it has a witness to each one.

Dora is highly efficient. Each step of the computation requires performing a small number of ZKBag operations, each of which has constant overhead. Looking ahead, we benchmark Dora in Section 8 and show that even on massive circuits (thousands of branches with thousands of gates each), proving each step of the RAM program takes only milliseconds.

3 Preliminaries

In this section, we recall some prelimary definitions. In Section 3.1, we present a definition of linearly homomorphic commitments. In Section 3.2, we recall the definition of a commit-and-prove zero-knowledge protocol. In Section 3.3, we provide a formal overview of relaxed R1CS [KST22]. In Section 3.4, we recall a construction of commit-and-prove ZK for R1CS (implicit in [KST22]). Finally, in Section 3.5 we recall the construction of Neff-style [Nef01] multi-set equality proofs.

Notation. Let t be the number of steps in the program trace, ℓ be the number of instructions in the processor circuit, m be the number of addresses in memory.

3.1 Linearly Homomorphic Commitments

Our construction makes use of a standard linearly homomorphic commitment primitive, which we define below. We intentionally give a general enough definition of this primitive that can capture both *interactive* instantiations (eg. VOLE-based [BMRS21]) and *non-interactive* instantiations (eg. Pedersen [Ped92]).

Definition 1 (Linearly Homomorphic Commitments)**.** *Linearly homomorphic commitments comprise of a tuple of four interactive protocols* $\pi^{\mathsf{LCom}} = (\pi^{\mathsf{LCom}}_{\mathsf{Setup}}, \pi^{\mathsf{LCom}}_{\mathsf{Commit}}, \pi^{\mathsf{LCom}}_{\mathsf{Open}}, \pi^{\mathsf{LCom}}_{\mathsf{Comb}})$ *between a Sender* Sen *and receiver* Rec *and a PPT algorithm* $\mathsf{Equiv}^{\mathsf{LCom}}$ *defined as follows:*

- $((\mathsf{pp}, \mathsf{skey}), (\mathsf{pp}, \mathsf{rkey})) \leftarrow \pi^{\mathsf{LCom}}_{\mathsf{Setup}}$*: The setup protocol generates any needed public parameters* pp*, a sender key* skey *as output for the sender and a receiver key* rkey *as output for the receiver.*
- $((\mathsf{com}, \mathsf{op}), (\mathsf{com})) \leftarrow \pi^{\mathsf{LCom}}_{\mathsf{Commit}}$*: The commit protocol takes the value* val *to be committed as input from the sender and outputs a commitment* com *to both the sender and the receiver. It additionally outputs* op *to the sender.*
- $((b), (\mathsf{val}')) \leftarrow \pi^{\mathsf{LCom}}_{\mathsf{Open}}$*: Both the sender and receiver invoke the opening protocol using a commitment* com *as input. The sender additionally inputs a value* val *committed inside this commitment and the associated opening information* op*. This protocol outputs a value* $\mathsf{val}' \in \{\mathsf{val}, \perp\}$ *to the receiver and a bit* $b \in \{0, 1\}$ *to the sender indicating whether or not* $\mathsf{val}' \stackrel{?}{=} \mathsf{val}$*.*
- $((\mathsf{com}, \mathsf{op}), (\mathsf{com})) \leftarrow \pi^{\mathsf{LCom}}_{\mathsf{Comb}}$*: The linear combination protocol takes* $(\mathsf{pp}, \mathsf{skey}, f_{\mathsf{lin}}, \mathsf{com}_1, \mathsf{op}_1, \mathsf{com}_2, \mathsf{op}_2)$ *as input from the sender and* $(\mathsf{pp}, \mathsf{rkey}, f_{\mathsf{lin}}, \mathsf{com}_1, , \mathsf{com}_2)$ *as input from the receiver. It computes the function* f_{lin} *on* com_1 *and* com_2 *and outputs the resulting new commitment* com *and its corresponding opening information* op*.*

- $\mathsf{op} \leftarrow \mathsf{Equiv}^{\mathsf{LCom}}(\mathsf{pp}, \mathsf{rkey}, \mathsf{com}, \mathsf{val})$*: The equivocation algorithm and outputs the new opening information* op *corresponding to* com *and* val.

We require that the commitment scheme satisfies hiding*, in the standard way. For* binding*, we assume that the commitment scheme has an extractor that can extract the val within a commitment. In addition to these standard properties, we assume that the* $\pi^{\mathsf{LCom}}_{\mathsf{Comb}}$ *algorithm allows the sender and receiver to perform linear operations over commitments and we assume that the receiver can always equivocate. Formally, these properties are defined as follows:*

1. ***Hiding:*** *Let* $((\mathsf{pp}, \mathsf{skey}), (\mathsf{pp}, \mathsf{rkey})) \leftarrow \pi^{\mathsf{LCom}}_{\mathsf{Setup}}\langle(\mathsf{Sen}(1^\lambda), \mathsf{Rec}(1^\lambda)\rangle$ *be an honest execution of the setup protocol. For any* $\mathsf{val}_1, \mathsf{val}_2 \in \mathcal{V}$*, the view of* Rec *remains computationally indistinguishable in the following two executions:*

$$\pi^{\mathsf{LCom}}_{\mathsf{Commit}}\langle\mathsf{Sen}(\mathsf{pp}, \mathsf{skey}, \mathsf{val}_1), \mathsf{Rec}(\mathsf{pp}, \mathsf{rkey})\rangle$$

$$\pi^{\mathsf{LCom}}_{\mathsf{Commit}}\langle\mathsf{Sen}(\mathsf{pp}, \mathsf{skey}, \mathsf{val}_2), \mathsf{Rec}(\mathsf{pp}, \mathsf{rkey})\rangle$$

2. ***Equivocation:*** *Let* $((\mathsf{pp}, \mathsf{skey}), (\mathsf{pp}, \mathsf{rkey})) \leftarrow \pi^{\mathsf{LCom}}_{\mathsf{Setup}}\langle(\mathsf{Sen}(1^\lambda), \mathsf{Rec}(1^\lambda)\rangle$ *be an honest execution of the setup protocol. The following holds* $\forall\ \mathsf{val} \in \mathcal{V}$ *and every honest execution of the commit protocol* $((\mathsf{com}, \mathsf{op}), (\mathsf{com})) \leftarrow \pi^{\mathsf{LCom}}_{\mathsf{Commit}}\langle\mathsf{Sen}(\mathsf{pp}, \mathsf{skey}, \mathsf{val}), \mathsf{Rec}(\mathsf{pp}, \mathsf{rkey})\rangle$*: if* $(\mathsf{val}', \mathsf{op}') \leftarrow \mathsf{Equiv}^{\mathsf{LCom}}(\mathsf{pp}, \mathsf{rkey}, \mathsf{com})$*, then for an honest sender and receiver,*

$$\Pr[((1), (\mathsf{val}')) \leftarrow \pi^{\mathsf{LCom}}_{\mathsf{Open}}\langle\mathsf{Sen}(\mathsf{pp}, \mathsf{skey}, \mathsf{com}, \mathsf{op}', \mathsf{val}'), \mathsf{Rec}(\mathsf{pp}, \mathsf{rkey}, \mathsf{com})\rangle] \geq 1 - \mathsf{neg}(\lambda)$$

3. ***Linear Homorphism:*** *Let* $((\mathsf{pp}, \mathsf{skey}), (\mathsf{pp}, \mathsf{rkey})) \leftarrow \pi^{\mathsf{LCom}}_{\mathsf{Setup}}\langle(\mathsf{Sen}(1^\lambda), \mathsf{Rec}(1^\lambda)\rangle$ *be an honest execution of the setup protocol. The following holds for all* $\mathsf{val}_1, \mathsf{val}_2 \in \mathcal{V}$*, every linear function* $f_{\mathsf{lin}} : \mathcal{V} \times \mathcal{V} \to \mathcal{V}$ *and all honest executions of the commit protocol* $(\forall\ i \in [2])\ ((\mathsf{com}_i, \mathsf{op}_i), (\mathsf{com}_i)) \leftarrow \pi^{\mathsf{LCom}}_{\mathsf{Commit}}\langle\mathsf{Sen}(\mathsf{pp}, \mathsf{skey}, \mathsf{val}_i), \mathsf{Rec}(\mathsf{pp}, \mathsf{rkey})\rangle$*: if*

$$((\mathsf{com}, \mathsf{op}), (\mathsf{com})) \leftarrow \pi^{\mathsf{LCom}}_{\mathsf{Comb}}\left\langle\mathsf{Sen}(\mathsf{pp}, \mathsf{skey}, f_{\mathsf{lin}}, \mathsf{com}_1, \mathsf{op}_1, \mathsf{com}_2, \mathsf{op}_2), \mathsf{Rec}(\mathsf{pp}, \mathsf{rkey}, f_{\mathsf{lin}}, \mathsf{com}_1, , \mathsf{com}_2)\right\rangle,$$

then for an honest sender and receiver,

$$\Pr[((1), (f_{\mathsf{lin}}(\mathsf{val}_1, \mathsf{val}_2))) \leftarrow \pi^{\mathsf{LCom}}_{\mathsf{Open}}\langle\mathsf{Sen}(\mathsf{pp}, \mathsf{skey}, \mathsf{com}, \mathsf{op}, f_{\mathsf{lin}}(\mathsf{val}_1, \mathsf{val}_2), \mathsf{Rec}(\mathsf{pp}, \mathsf{rkey}, \mathsf{com})\rangle] \geq 1 - \mathsf{neg}(\lambda)$$

4. ***Binding/Extraction:*** *Let* $((\mathsf{pp}, \mathsf{skey}), (\mathsf{pp}, \mathsf{rkey})) \leftarrow \pi^{\mathsf{LCom}}_{\mathsf{Setup}}\langle(\mathsf{Sen}(1^\lambda), \mathsf{Rec}(1^\lambda)\rangle$ *be an honest execution of the setup protocol. There exists an extractor* $\mathcal{E}$*, such that for any PPT adversary* $\mathcal{A}$ *and for any* com *such that* $((\cdot), (\mathsf{com})) \leftarrow \pi^{\mathsf{LCom}}_{\mathsf{Commit}}\langle\mathcal{A}(\mathsf{pp}, \mathsf{skey}, \cdot), \mathsf{Rec}(\mathsf{pp}, \mathsf{rkey})\rangle$*, then* $(\mathsf{val}) \leftarrow \mathcal{E}^{\mathcal{O}(\mathcal{A})}(\mathsf{pp})$ *such that for any honest receiver and* $\mathsf{val} \neq \mathsf{val}' \neq \bot$*, it holds that*

$$\Pr[((\cdot), (\mathsf{val}')) \leftarrow \pi^{\mathsf{LCom}}_{\mathsf{Open}}\langle\mathcal{A}(\mathsf{pp}, \mathsf{skey}, \mathsf{com}, \cdot), \mathsf{Rec}(\mathsf{pp}, \mathsf{rkey}, \mathsf{com})\rangle] \leq \mathsf{neg}(\lambda)$$

Short-Hand Notation. For simplicity, we use the notation $[\![v]\!]$ denotes a commitment to some value $\overrightarrow{v}$. We often abuse notation and use $[\![\overrightarrow{x}]\!]$ to denote a linearly homomorphic commitment to a vector of elements in $\overrightarrow{x} \in \mathbb{F}^*$. We use linear arithmetic operations as a short-hand for $\pi^{\mathsf{LCom}}_{\mathsf{Comb}}$, e.g., $[\![\mathsf{val}]\!] = c_1 \cdot [\![\mathsf{val}_1]\!] + [\![\mathsf{val}_2]\!]$, where c_1 is some public value. Finally, we remark that the by default, the above definition of $\pi^{\mathsf{LCom}}_{\mathsf{Commit}}$ is presented for *private commitments*, i.e., it only takes the value to be committed as input from the sender. However, it can easily be adapted to allow for *public commitments*, where both the sender and receiver have access to the value being committed. It that case, we assume that in addition to taking val as input from both parties, $\pi^{\mathsf{LCom}}_{\mathsf{Commit}}$ is run on shared randomness between the sender and receiver.

3.2 Commit-and-Prove Zero-Knowledge

Both our final construction Dora and our subprotocol for handling processor instructions are custom-designed commit-and-prove style zero-knowledge for specific languages. In this section, we recall the definition of this primitive. We assume that the commitments in this definition were computed using inearly homomorphic commitments defined in Section 3.1.

Definition 2 (LinCom-Based Commit-and-Prove ZK)**.** *LinCom-based commit-and-prove zero-knowledge proof system for an NP-relation $\mathcal{R}$, comprises of a tuple of 3 interactive protocols $(\pi_{\mathsf{Setup}}, \pi_{\mathsf{Proof}}, \pi_{\mathsf{Verify}})$ between the sender and receiver defined as follows:*

- $((\mathsf{pp}, \mathsf{skey}), (\mathsf{pp}, \mathsf{rkey})) \leftarrow \pi^{\mathsf{ZK}}_{\mathsf{Setup}}$*:The setup protocol generates any needed public parameters* pp*, a sender key* skey *as output for the sender/prover and a receiver key* rkey *as output for the receiver/verifier.*
- $((\mathsf{Proof}^{\mathsf{ZK}}, \mathsf{st}), (\mathsf{Proof}^{\mathsf{ZK}})) \leftarrow \pi^{\mathsf{ZK}}_{\mathsf{Prove}}$*: The prove protocol takes as input* $(\mathsf{pp}, \mathsf{skey}, \overrightarrow{x}, \mathsf{com}, \overrightarrow{\mathsf{op}}, \overrightarrow{w})$ *from the sender/prover and* $(\mathsf{pp}, \mathsf{rkey}, \overrightarrow{x}, [\![\overrightarrow{w}]\!])$ *from the receiver/verifier. It outputs a proof* $\mathsf{Proof}^{\mathsf{ZK}}$ *that allows the prover/sender to convince the receiver/verifier that it knows $\overrightarrow{w}, \overrightarrow{\mathsf{op}}$ such that they are a valid opening for $[\![\overrightarrow{w}]\!]$ and $\overrightarrow{w}$ is a valid witness for statement $\overrightarrow{x}$. This protocol may additionally output some secret state* st *for the sender/prover.*
- $((b), (b)) \leftarrow \pi^{\mathsf{ZK}}_{\mathsf{Verify}}$*: The verify protocol takes as input* $(\mathsf{pp}, \mathsf{skey}, \mathsf{Proof}^{\mathsf{ZK}}, \mathsf{st}, \overrightarrow{x})$ *from the sender/prover and* $(\mathsf{pp}, \mathsf{rkey}, \mathsf{Proof}^{\mathsf{ZK}}, \overrightarrow{x})$ *from the receiver/verifier and outputs a bit $b \in \{0, 1\}$, based on whether or not the proof* $\mathsf{Proof}^{\mathsf{ZK}}$ *verifies.*

We require the above protocols to satisfy the standard notions of correctness*,* zero-knowledge *and* knowledge soundness.

3.3 Relaxed R1CS

In this work, we use *Relaxed R1CS*, a generalization of R1CS introduced by Kothapalli, Setty and Tzialla [KST22]:

Definition 3 (Relaxed R1CS, [KST22])**.** *A relaxed R1CS (Rank-1 Constraint System) [KST22] is defined by three matrixes $\mathbf{A}, \mathbf{B}, \mathbf{C} \in \mathbb{F}^{m \times m}$. A witness* w *satisfies an instance $(\overrightarrow{\mathsf{e}}, \overrightarrow{\mathsf{x}}, \mathsf{u})$ iff. the "extended witness" $\overrightarrow{\mathsf{z}} = \overrightarrow{\mathsf{w}} \| \overrightarrow{\mathsf{x}} \| \mathsf{u} \in \mathbb{F}^m$ satisfies: $(\mathbf{A} \cdot \overrightarrow{\mathsf{z}}) \circ (\mathbf{B} \cdot \overrightarrow{\mathsf{z}}) = \mathsf{u} \cdot (\mathbf{C} \cdot \overrightarrow{\mathsf{z}}) + \overrightarrow{\mathsf{e}}$. For ease of notation, refer to Relaxed R1CS instances by their extended witness $\overrightarrow{\mathsf{z}}$ and error term $\overrightarrow{\mathsf{e}}$, which in turn defines $\overrightarrow{\mathsf{w}}, \overrightarrow{\mathsf{x}}$, and* u.

One valuable feature of Relaxed R1CS instances, as noted by [KST22], is that they can be "folded." That is, given two Relaxed R1CS instances $(\overrightarrow{\mathsf{z}_1}, \overrightarrow{\mathsf{e}_1})$ and $(\overrightarrow{\mathsf{z}_2}, \overrightarrow{\mathsf{e}_2})$ and a randomly sampled $r \in \mathbb{F}$, we can define a new instance $(\overrightarrow{\mathsf{z}}, \overrightarrow{\mathsf{e}})$ as:

$$\overrightarrow{\mathsf{e}} = \overrightarrow{\mathsf{e}_1} + r \cdot \overrightarrow{T} + r^2 \cdot \overrightarrow{\mathsf{e}_2}, \qquad \mathsf{u} = \mathsf{u}_1 + r \cdot \mathsf{u}_2 \qquad \overrightarrow{\mathsf{z}} = \overrightarrow{\mathsf{z}_1} + r \cdot \overrightarrow{\mathsf{z}_2}$$

where

$$\overrightarrow{T} = \mathbf{A} \cdot \overrightarrow{\mathsf{z}_1} \circ \mathbf{B} \cdot \overrightarrow{\mathsf{z}_2} + \mathbf{A} \cdot \overrightarrow{\mathsf{z}_2} \circ \mathbf{B} \cdot \overrightarrow{\mathsf{z}_1} - \mathsf{u}_1 \cdot \mathbf{C} \cdot \overrightarrow{\mathsf{z}_2} - \mathsf{u}_2 \cdot \mathbf{C} \cdot \overrightarrow{\mathsf{z}_1}$$

Importantly, this folding process is *sound*, in that if either $(\overrightarrow{\mathsf{z}_1}, \overrightarrow{\mathsf{e}_1})$ or $(\overrightarrow{\mathsf{z}_2}, \overrightarrow{\mathsf{e}_2})$ are not satisfied, then $(\overrightarrow{\mathsf{z}}, \overrightarrow{\mathsf{e}})$ is also unsatisfied with high probability (over the choice of r).

An additional fact about the folding scheme above (not directly used in Nova [KST22]) is that the folding *only depends on the dimensions of* $\mathbf{A}$, $\mathbf{B}$ *and* $\mathbf{C}$. This means that we can have the verifier "fold" two committed instances pairs without revealing the relation these instances belong. This will be crucial as we will be executing the folder "obliviously," in that only the prover will know which instance is being considered.

Remark (*R1CS is a Special Case of Relaxed R1CS).* Note that regular R1CS is captured as the special case of Definition 3 where $\overrightarrow{\mathsf{e}} = \overrightarrow{0} \in \mathbb{F}^m$ and $\mathsf{u} = 1$. Throughout the section, to simplify notation, we will refer to relaxed R1CS instances by their error term $\overrightarrow{\mathsf{e}} \in \mathbb{F}^m$ and extended witness $\overrightarrow{\mathsf{z}} \in \mathbb{F}^m$; which define $\overrightarrow{\mathsf{w}}, \overrightarrow{\mathsf{x}}, \mathsf{u}$.

3.4 Commit-and-Prove ZK for R1CS

Next, we recall a simple Σ-protocol for R1CS-satisfiability. This protocol is derived directly from the Nova [KST22] IVC scheme. This protocol satisfies all the properties that we need from a commit and prove zero-knowledge protocol defined in Section 3.2. Let $(\mathbf{A}, \mathbf{B}, \mathbf{C})$ be an R1CS instance. Given a commitment $[\![\overrightarrow{\mathsf{z}}]\!]$, computed using a linearly homomorphic commitment (see Section 3.1), the prover wants to convince the verifier that the value $\overrightarrow{\mathsf{z}} = \overrightarrow{\mathsf{w}} \| \overrightarrow{\mathsf{x}} \| \mathsf{u}$ committed inside this commitment is a valid extended witness for $(\mathbf{A}, \mathbf{B}, \mathbf{C})$. The setup algorithm $\pi^{\mathsf{ZK}}_{\mathsf{Setup}}$ of this proof system is the same as the setup of the above linearly homomorphic commitment scheme. We now describe the $\pi^{\mathsf{ZK}}_{\mathsf{Prove}}$ and $\pi^{\mathsf{ZK}}_{\mathsf{Verify}}$ protocols.

- Prover samples a random satisified relaxed R1CS instance as follows:
  - Sample $\overrightarrow{\mathsf{z}_0} \leftarrow\$ \mathbb{F}^m$ and parse $\overrightarrow{\mathsf{z}_0} = \overrightarrow{\mathsf{w}_0} \| \overrightarrow{\mathsf{x}_0} \| \mathsf{u}_0$.
  - Set $\overrightarrow{L} \leftarrow (\mathbf{A} \cdot \overrightarrow{\mathsf{z}_0}) \circ (\mathbf{B} \cdot \overrightarrow{\mathsf{z}_0})$, $\overrightarrow{R} \leftarrow \mathsf{u}_0 \cdot (\mathbf{C} \cdot \overrightarrow{\mathsf{z}_0})$ and $\overrightarrow{\mathsf{e}_0} \leftarrow \overrightarrow{L} - \overrightarrow{R}$
- Prover then computes the cross terms:

$$\overrightarrow{t_1} \leftarrow \mathbf{A} \cdot \overrightarrow{\mathsf{z}} \circ \mathbf{B}_i \cdot \overrightarrow{\mathsf{z}_0} + \mathbf{A} \cdot \overrightarrow{\mathsf{z}_0} \circ \mathbf{B}_i \cdot \overrightarrow{\mathsf{z}}$$

$$\overrightarrow{t_2} \leftarrow \mathsf{u} \cdot \mathbf{C} \cdot \overrightarrow{\mathsf{z}_0} + \mathsf{u}_0 \cdot \mathbf{C} \cdot \overrightarrow{\mathsf{z}}$$

$$\overrightarrow{T} \leftarrow \overrightarrow{t_1} - \overrightarrow{t_2}$$

- Prover and verifier use $\pi^{\mathsf{LCom}}_{\mathsf{Commit}}$ to compute commitment-opening pairs $((\llbracket T \rrbracket, \mathsf{op}_T), (\llbracket T \rrbracket))$, $(\llbracket \mathsf{z}_0 \rrbracket, \mathsf{op}_{\mathsf{z}_0})$ and $(\llbracket \mathsf{z}_0 \rrbracket, \mathsf{op}_{\mathsf{e}_0})$.
- The verifier then samples and sends $r \leftarrow\$ \mathbb{F}$.
- Prover uses $\pi^{\mathsf{LCom}}_{\mathsf{Comb}}, \pi^{\mathsf{LCom}}_{\mathsf{Open}}$ to open the following linear combinations of the two instances:
  - Let $\overrightarrow{\mathsf{e}'}$ be the opened value associated with the commitment $(r \cdot \left\llbracket \overrightarrow{T} \right\rrbracket + r^2 \cdot \llbracket \overrightarrow{\mathsf{e}_0} \rrbracket)$
  - Let $\overrightarrow{\mathsf{z}'}$ be the opened value associated with the commitment $(\overrightarrow{\mathsf{z}} + r \cdot \overrightarrow{\mathsf{z}_0})$
- Finally, if the above openings are valid, the verifier checks: $\left(\mathbf{A} \cdot \overrightarrow{\mathsf{z}'}\right) \circ \left(\mathbf{B} \cdot \overrightarrow{\mathsf{z}'}\right) =^{?} = \mathsf{u}' \cdot \mathbf{C} \cdot \overrightarrow{\mathsf{z}'} + \overrightarrow{\mathsf{e}'}$, where $\mathsf{u}' = \mathsf{u} + r \cdot \mathsf{u}_0$.

3.5 Multi-Set Equality Proofs

In our construction of ZKBag, we leverage an efficient set equality proof (also referred to as a permutation proof). In our concrete instantiation of Dora, we use the simple Bayer-Groth style proof. To the best of our knowledge, this construction was first documented in [Nef01] and has subsequently been independently discovered in many works [BG12, FKL+21]. Given 2 sets of commitments, $\mathcal{S}_1 = (\llbracket \overrightarrow{a}_1 \rrbracket, \ldots, \llbracket \overrightarrow{a}_k \rrbracket)$ and $\mathcal{S}_2 = (\left\llbracket \overrightarrow{b}_1 \right\rrbracket, \ldots, \left\llbracket \overrightarrow{b}_k \right\rrbracket)$, the multi-set equality proof can be viewed as a commit-and-prove zero-knowledge protocol (say $(\pi^{\mathsf{ZKMultiSet}}_{\mathsf{Setup}}, \pi^{\mathsf{ZKMultiSet}}_{\mathsf{Prove}}, \pi^{\mathsf{ZKMultiSet}}_{\mathsf{Verify}})$) for the following relation: *there exists a permutation p, such that* $p(\overrightarrow{a}_1, \ldots, \overrightarrow{a}_k) = \overrightarrow{b}_1, \ldots, \overrightarrow{b}_k$.

We now recall this well-known Bayer-Groth style [BG12] shuffle proof. We assume that all commitments were computed using linearly homomorphic commitments from Section 3.1. This is the only component in our construction that (black-box) relies on a general proof system – let $(\pi^{\mathsf{ZK}}_{\mathsf{Setup}}, \pi^{\mathsf{ZK}}_{\mathsf{Prove}}, \pi^{\mathsf{ZK}}_{\mathsf{Verify}})$ be the commit and prove zero-knowledge protocol for general R1CS satisfiability from Section 3.4. The setup algorithm $\pi^{\mathsf{ZKMultiSet}}_{\mathsf{Setup}}$ of this proof system is the same as the setup of the above linearly homomorphic commitment scheme. We now describe the $\pi^{\mathsf{ZKMultiSet}}_{\mathsf{Prove}}$ and $\pi^{\mathsf{ZKMultiSet}}_{\mathsf{Verify}}$ protocols.

- Verifier samples random field elements $u, v \leftarrow\$ \mathbb{F}$, and sends them to the prover.
- For each $i \in [k]$, both the prover and verifier use $\pi^{\mathsf{LCom}}_{\mathsf{Comb}}$ to compute

$$\llbracket \alpha_i \rrbracket = \left\langle (1, u^2, \ldots, u^{k-1}), \llbracket \overrightarrow{a_i} \rrbracket \right\rangle$$

$$\llbracket \beta_i \rrbracket = \left\langle (1, u^2, \ldots, u^{k-1}), \left\llbracket \overrightarrow{b_i} \right\rrbracket \right\rangle$$

- Finally, the prover uses $(\pi^{\mathsf{ZK}}_{\mathsf{Setup}}, \pi^{\mathsf{ZK}}_{\mathsf{Prove}}, \pi^{\mathsf{ZK}}_{\mathsf{Verify}})$ to convince the verifier that $\prod_{i \in [k]} (v - \llbracket \alpha_i \rrbracket) = \prod_{i \in [k]} (v - \llbracket \beta_i \rrbracket)$.

4 Zero-Knowledge Bag

As discussed in Section 2.2, the heart of Dora is a zero-knowledge bag (ZKBag) protocol. This cryptographic object is analogous to a physical bag into which the prover and verifier place wrapped objects. The critical properties of the protocol are equivalent to the physical properties that such a bag would possess: only objects previously put into the bag can be removed, and the bag itself hides the correspondence between the order in which objects are inserted and removed. In some sense, the zero-knowledge bag can be seen as a "slow moving" shuffle proof augmented with a sense of time.

4.1 Defining ZKBag

Definition 4 (LinCom-Based Zero-Knowledge Bag)**.** *A ZKBag is parameterized by a linearly homomorphic commitment scheme, and as such we call the resulting cryptographic primitive a LinCom-Based ZKBag. A LinCom-Based ZKBag comprises of a tuple of 5 interactive protocols* $(\pi^{\mathsf{ZKBag}}_{\mathsf{Setup}}, \pi^{\mathsf{ZKBag}}_{\mathsf{Init}}, \pi^{\mathsf{ZKBag}}_{\mathsf{Insert}}, \pi^{\mathsf{ZKBag}}_{\mathsf{Remove}}, \pi^{\mathsf{ZKBag}}_{\mathsf{VerEmpty}})$ *between the sender and receiver. We omit formally writing out the inputs to each protocol for space, but they are included in the headers of Figure 1:*

- $((\mathsf{pp}, \mathsf{skey}), (\mathsf{pp}, \mathsf{rkey})) \leftarrow \pi^{\mathsf{ZKBag}}_{\mathsf{Setup}}$*: The setup protocol generates any needed public parameters* pp*, generates a sender key* skey *as output for the sender and a receiver key* rkey *as output for the receiver.*
- $((\mathsf{bag}, \mathsf{state}), (\mathsf{bag})) \leftarrow \pi^{\mathsf{ZKBag}}_{\mathsf{Init}}$ *: The parties take the output of* $\pi^{\mathsf{ZKBag}}_{\mathsf{Setup}}$ *as input and initialize the ZKBag. The sender and receiver each maintain some joint information* bag *and the sender maintains some secret information* state*.*
- $((\mathsf{bag}', \mathsf{state}'), (\mathsf{bag}')) \leftarrow \pi^{\mathsf{ZKBag}}_{\mathsf{Insert}}$ *: The parties take in the current state of the bag* $((\mathsf{bag}, \mathsf{state}), (\mathsf{bag}))$ *and a commitment* $[\![\overrightarrow{\mathsf{val}}]\!]$*. Additionally, the sender provides a valid opening to the commitment* $(\overrightarrow{\mathsf{val}}, \mathsf{op})$*. This updates the state of the bag held by both the sender and the receiver.*
- $((\mathsf{bag}', \mathsf{state}'), (\mathsf{bag}')) \leftarrow \pi^{\mathsf{ZKBag}}_{\mathsf{Remove}}$ *: The parties take in the current state of the bag* $((\mathsf{bag}, \mathsf{state}), (\mathsf{bag}))$ *and a commitment* $[\![\overrightarrow{\mathsf{val}}]\!]$*. Additionally, the sender provides a valid opening to the commitment* $(\overrightarrow{\mathsf{val}}, \mathsf{op})$*. This updates the state of the bag held by both the sender and the receiver.*
- $((b), (b)) \leftarrow \pi^{\mathsf{ZKBag}}_{\mathsf{VerEmpty}}$ *: The parties take in the current state of the bag* $((\mathsf{bag}, \mathsf{state}), (\mathsf{bag}))$ *and check if the bag is empty. This outputs a bit* b *to the sender and the receiver.*

We define 3 properties of these algorithms: correctness*,* knowledge soundness*, and* zero-knowledge*.*

1. Correctness: *Correctness considers an interaction between the sender and receiver in which they run setup and initialize. After this first phase, the sender and receiver run an arbitrary sequence if inserts and removes. If there is a one-to-one correspondence between inserts and removes such that the remove always comes after the corresponding insert and the values in each corresponding pair are for the same values, then a call to* $\pi^{\mathsf{ZKBag}}_{\mathsf{VerEmpty}}$ *will return* 1*.*

   Formally speaking, let $((\mathsf{pp}, \mathsf{skey}), (\mathsf{pp}, \mathsf{rkey})) \leftarrow \pi^{\mathsf{ZKBag}}_{\mathsf{Setup}}\langle(\mathsf{Sen}(1^\lambda), \mathsf{Rec}(1^\lambda)\rangle$*,* $((\mathsf{bag}, \mathsf{state}), (\mathsf{bag})) \leftarrow \pi^{\mathsf{ZKBag}}_{\mathsf{Init}}\langle\mathsf{Sen}(\mathsf{pp}, \mathsf{skey}), \mathsf{Rec}(\mathsf{pp}, \mathsf{rkey})\rangle$ *be honest executions of the setup and initialization protocols. For any* $n \in \mathsf{poly}(\lambda)$*,* $\mathsf{val}_1, \ldots, \mathsf{val}_n \in \mathcal{V}$ *and any sequence of* $2n$ *executions of the insert and remove protocols such that for each* $i \in [n]$*, a protocol of the form* $\pi^{\mathsf{ZKBag}}_{\mathsf{Remove}}\langle\mathsf{Sen}(\cdots, \mathsf{com}_i, \mathsf{op}_i \mathsf{val}_i), \mathsf{Rec}(\cdots, \mathsf{com}_i)\rangle$ *only appears after* $\pi^{\mathsf{ZKBag}}_{\mathsf{Insert}}\langle\mathsf{Sen}(\cdots, \mathsf{com}'_i, \mathsf{op}'_i \mathsf{val}_i), \mathsf{Rec}(\cdots, \mathsf{com}'_i)\rangle$ *in the sequence and each of these appear exactly once, it holds that:*

$$\Pr\left[((1), (1)) \leftarrow \pi^{\mathsf{ZKBag}}_{\mathsf{VerEmpty}}\langle\mathsf{Sen}(\mathsf{pp}, \mathsf{skey}, \mathsf{bag}, \mathsf{state}), \mathsf{Rec}(\mathsf{pp}, \mathsf{rkey}, \mathsf{bag})\rangle\right] \geq 1 - \mathsf{neg}(\lambda)$$

   Here for each $i \in [n]$*,* com_i *and* com'_i *are commitments of the form* $((\mathsf{com}_i, \mathsf{op}_i), (\mathsf{com}_i)) \leftarrow \pi^{\mathsf{LCom}}_{\mathsf{Commit}}\langle\mathsf{Sen}(\mathsf{pp}, \mathsf{skey}, \mathsf{val}_i), \mathsf{Rec}(\mathsf{pp}, \mathsf{rkey})\rangle$ *and* $((\mathsf{com}'_i, \mathsf{op}'_i), (\mathsf{com}'_i)) \leftarrow \pi^{\mathsf{LCom}}_{\mathsf{Commit}}\langle\mathsf{Sen}(\mathsf{pp}, \mathsf{skey}, \mathsf{val}'_i), \mathsf{Rec}(\mathsf{pp}, \mathsf{rkey})\rangle$*.*

2. Knowledge Soundness: *Knowledge soundness intuitively says that a malicious sender cannot convince the receiver that the bag is empty after an interaction unless all the restrictions on the interaction from* correctness *hold and the*

bag truly is empty. We formalize this by saying that there exists an extractor that can extract the values used in the insertions and removals, such that (as above) there is a one-to-one correspondence between inserts and removes such that the remove always comes after the corresponding insert and the values in each corresponding pair are for the same values.

Formally speaking, let $((\mathsf{pp}, \mathsf{skey}), (\mathsf{pp}, \mathsf{rkey})) \leftarrow \pi^{\mathsf{ZKBag}}_{\mathsf{Setup}}\langle(\mathsf{Sen}(1^\lambda), \mathsf{Rec}(1^\lambda)\rangle$ *be an honest execution of the setup protocol. There exists an extractor* $\mathcal{E}$ *such that, for any PPT adversary* $\mathcal{A}$*, any* $n \in \mathsf{poly}(\lambda)$*, any execution of the initialization protocol of the form* $((\cdots), (\mathsf{bag}_0)) \leftarrow \pi^{\mathsf{ZKBag}}_{\mathsf{Init}}\langle\mathcal{A}(\mathsf{pp}, \mathsf{skey}), \mathsf{Rec}(\mathsf{pp}, \mathsf{rkey})\rangle$*, and any sequence of* $2n$ *protocol executions* $\left(((\cdots), (\mathsf{bag}_i)) \leftarrow \pi_{\mathsf{Update}_i}\langle\mathcal{A}(\mathsf{pp}, \mathsf{skey}, \mathsf{com}_i \cdots), \mathsf{Rec}(\mathsf{pp}, \mathsf{rkey}, \mathsf{bag}_{i-1}, \mathsf{com}_i)\rangle\right)_{i\in[2n]}$ *where each* com_i *is the result of invoking*

$$((\mathsf{com}_i, \mathsf{op}_i), (\mathsf{com}_i)) \leftarrow \pi^{\mathsf{LCom}}_{\mathsf{Commit}}\left\langle\mathcal{A}(\mathsf{pp}, \mathsf{skey}), \mathsf{Rec}(\mathsf{pp}, \mathsf{rkey})\right\rangle,$$

and where for each $i \in [2n]$, $\mathsf{Update}_i \in \{\mathsf{Insert}, \mathsf{Remove}\}$*, if it holds that,*

$$((\cdot), (1)) \leftarrow \pi^{\mathsf{ZKBag}}_{\mathsf{VerEmpty}}\langle\mathcal{A}(\mathsf{pp}, \mathsf{skey}, \mathsf{bag}_{2n}), \mathsf{Rec}(\mathsf{pp}, \mathsf{rkey}, \mathsf{bag}_{2n})\rangle$$

then $(\mathsf{val}_1, \ldots, \mathsf{val}_{2n}) \leftarrow \mathcal{E}^{\mathcal{O}(\mathcal{A})}(\mathsf{pp})$*, such that if* $\mathsf{Index}_{\mathsf{Insert}}$ *and* $\mathsf{Index}_{\mathsf{Remove}}$ *denote the values of* i *corresponding to insertions and removals, then*

$$\Pr\left[\exists \text{ a bijection } f : \mathsf{Index}_{\mathsf{Insert}} \to \mathsf{Index}_{\mathsf{Remove}}, \text{ s.t., } \forall i \in \mathsf{Index}_{\mathsf{Insert}}, (f(i) > i) \wedge \left(\mathsf{val}_i = \mathsf{val}_{f(i)}\right)\right] \geq 1 - \mathsf{neg}(\lambda)$$

and for all $i \in [2n]$*, any honest receiver* Rec*, and computationally bounded adversary* $\mathcal{A}$*, and any* $\mathsf{val}_i \neq \mathsf{val}'_i \neq \bot$*, it holds that*

$$\Pr[((\cdot), (\mathsf{val}'_i)) \leftarrow \pi^{\mathsf{LCom}}_{\mathsf{Open}}\langle\mathcal{A}(\mathsf{pp}, \mathsf{skey}, \mathsf{com}, \cdot), \mathsf{Rec}(\mathsf{pp}, \mathsf{rkey}, \mathsf{com})\rangle] \leq \mathsf{neg}(\lambda)$$

3. Zero-Knowledge: *Zero-knowledge says that the receiver learns nothing about the values inserted and removed, beyond the fact that the limitations from* correctness *are satisfied. We formalize this by saying that the view of the receiver in an honest interaction with the sender is computationally indistinguishable from an interaction with a simulator that does not know the values inserted or removed from the bag.*

   Formally speaking, the exists a simulator $\mathsf{Sim} = (\mathsf{Sim}_{\mathsf{Setup}}, \mathsf{Sim}_{\mathsf{Init}}, \mathsf{Sim}_{\mathsf{Insert}}, \mathsf{Sim}_{\mathsf{Remove}}, \mathsf{Sim}_{\mathsf{VerEmpty}})$*, such that for any* $n \in \mathsf{poly}(\lambda)$*, the the view of* Rec *in the following sequence of protocol executions*

$$((\mathsf{pp}, \mathsf{skey}), (\mathsf{pp}, \mathsf{rkey})) \leftarrow \pi^{\mathsf{ZKBag}}_{\mathsf{Setup}}\left\langle\mathsf{Sen}(1^\lambda), \mathsf{Rec}(1^\lambda)\right\rangle$$

$$((\mathsf{bag}_0, \mathsf{state}_0), (\mathsf{bag}_0)) \leftarrow \pi^{\mathsf{ZKBag}}_{\mathsf{Init}}\left\langle\mathsf{Sen}(\mathsf{pp}, \mathsf{skey}), \mathsf{Rec}(\mathsf{pp}, \mathsf{rkey})\right\rangle$$

   For each $i \in [2n]$ *and arbitrary* val_i*:*

$$((\mathsf{com}_i, \mathsf{op}_i), (\mathsf{com}_i)) \leftarrow \pi^{\mathsf{LCom}}_{\mathsf{Commit}}\left\langle\mathsf{Sen}(\mathsf{pp}, \mathsf{skey}, \mathsf{val}_i), \mathsf{Rec}(\mathsf{pp}, \mathsf{rkey})\right\rangle,$$

$$((\mathsf{bag}_i, \mathsf{state}_i), (\mathsf{bag}_i)) \leftarrow \pi^{\mathsf{ZKBag}}_{\mathsf{Update}_i}\left\langle\mathsf{Sen}(\mathsf{pp}, \mathsf{skey}, \mathsf{bag}_{i-1}, \mathsf{state}_{i-1}, \mathsf{com}_i, \mathsf{op}_i, \mathsf{val}_i), \mathsf{Rec}(\mathsf{pp}, \mathsf{rkey}, \mathsf{bag}_{i-1}, \mathsf{com}_i)\right\rangle,$$

   where $\mathsf{Update}_i \in \{\mathsf{Insert}, \mathsf{Remove}\}$*. And finally,*

$$((1), (1)) \leftarrow \pi^{\mathsf{ZKBag}}_{\mathsf{VerEmpty}}\left\langle\mathsf{Sen}(\mathsf{pp}, \mathsf{skey}, \mathsf{bag}_{2n}, \mathsf{state}_{2n}), \mathsf{Rec}(\mathsf{pp}, \mathsf{rkey}, \mathsf{bag}_{2n})\right\rangle$$

   is computationally indistinguishable from its view in the following sequence of protocol executions. For readability, we omit the state passing between the interactions, but assume that each part of the simulator and the receiver can pass arbitrary state:

$$\langle(\mathsf{Sim}_{\mathsf{Setup}}(1^\lambda) \leftrightarrow \mathsf{Rec}(1^\lambda)\rangle$$

$$\langle(\mathsf{Sim}_{\mathsf{Init}}(1^\lambda) \leftrightarrow \mathsf{Rec}(1^\lambda)\rangle$$

   For each $i \in [2n]$*:*

$$((\mathsf{com}_i, \mathsf{op}_i), (\mathsf{com}_i)) \leftarrow \pi^{\mathsf{LCom}}_{\mathsf{Commit}}\left\langle\mathsf{Sim}(\mathsf{pp}, \mathsf{skey}, 0), \mathsf{Rec}(\mathsf{pp}, \mathsf{rkey})\right\rangle,$$

$$\langle(\mathsf{Sim}_{\mathsf{Update}_i}(1^\lambda, \mathsf{com}_i, \mathsf{op}_i) \leftrightarrow \mathsf{Rec}(1^\lambda, \mathsf{com}_i)\rangle$$

   $\mathsf{Update}_i \in \{\mathsf{Insert}, \mathsf{Remove}\}$*. And finally,*

$$\langle(\mathsf{Sim}_{\mathsf{VerEmpty}}(1^\lambda) \leftrightarrow \mathsf{Rec}(1^\lambda)\rangle$$

4.2 Realizing ZKBag

$((\mathsf{pp}, \mathsf{skey}), (\mathsf{pp}, \mathsf{rkey})) \leftarrow \pi^{\mathsf{ZKBag}}_{\mathsf{Setup}}\langle(\mathsf{Sen}(1^\lambda), \mathsf{Rec}(1^\lambda)\rangle$

- Sen and Rec invoke $((\mathsf{pp}^{\mathsf{LCom}}, \mathsf{skey}^{\mathsf{LCom}}), (\mathsf{pp}^{\mathsf{LCom}}, \mathsf{rkey}^{\mathsf{LCom}})) \leftarrow \pi^{\mathsf{LCom}}_{\mathsf{Setup}}\langle(\mathsf{Sen}(1^\lambda), \mathsf{Rec}(1^\lambda)\rangle$
- Output $(\mathsf{pp} = \mathsf{pp}^{\mathsf{LCom}}, \mathsf{skey} = \mathsf{skey}^{\mathsf{LCom}})$ to Sen and $(\mathsf{pp} = \mathsf{pp}^{\mathsf{LCom}}, \mathsf{rkey} = \mathsf{rkey}^{\mathsf{LCom}})$ to Rec.

$((\mathsf{bag}, \mathsf{state}), (\mathsf{bag})) \leftarrow \pi^{\mathsf{ZKBag}}_{\mathsf{Init}}\langle\mathsf{Sen}(\mathsf{pp}, \mathsf{skey}), \mathsf{Rec}(\mathsf{pp}, \mathsf{rkey})\rangle$

- Sen and Rec each initialize an empty list of inserted elements $\mathcal{I} \leftarrow \emptyset$, an empty list of removed elements $\mathcal{R} \leftarrow \emptyset$ and a counter $\mathsf{cnt} \leftarrow 0$. Additionally, Sen initializes a map $\mathbb{B} \leftarrow \emptyset$.
- Output $((\mathcal{I}, \mathcal{R}), \mathbb{B})$ to Sen and $(\mathcal{I}, \mathcal{R})$ to Rec.

$((\mathsf{bag}', \mathsf{state}'), (\mathsf{bag}')) \leftarrow \pi^{\mathsf{ZKBag}}_{\mathsf{Insert}}\langle\mathsf{Sen}(\mathsf{pp}, \mathsf{skey}, \mathsf{bag}, \mathsf{state}, \left[\!\left[\overrightarrow{\mathsf{val}}\right]\!\right], \mathsf{op}, \mathsf{val}), \mathsf{Rec}(\mathsf{pp}, \mathsf{rkey}, \mathsf{bag}, \left[\!\left[\overrightarrow{\mathsf{val}}\right]\!\right])\rangle$

- Rec samples $\mathsf{tag} \leftarrow\!\!\$\ \mathbb{F}$ and sends it to Sen.
- Sen and Rec invoke $((\llbracket \mathsf{tag} \rrbracket, \cdot), (\llbracket \mathsf{tag} \rrbracket)) \leftarrow \pi^{\mathsf{LCom}}_{\mathsf{Commit}}\langle\mathsf{Sen}(\mathsf{pp}, \mathsf{skey}, \mathsf{tag}), \mathsf{Rec}(\mathsf{pp}, \mathsf{rkey}, \mathsf{tag})\rangle$ on shared randomness.
- They add the following tuple to the list of inserted elements: $\mathcal{I} \leftarrow \mathcal{I} \cup (\llbracket \mathsf{tag} \rrbracket \parallel \left[\!\left[\overrightarrow{\mathsf{val}}\right]\!\right])$
- Finally, Sen adds a new counter and tag for the value to the map $\mathbb{B}[\mathsf{val}].\mathsf{Push}(\mathsf{tag})$
- Output $((\mathcal{I}, \mathcal{R}), \mathbb{B})$ to Sen and $(\mathcal{I}, \mathcal{R})$ to Rec.

$((\mathsf{bag}', \mathsf{state}'), (\mathsf{bag}')) \leftarrow \pi^{\mathsf{ZKBag}}_{\mathsf{Remove}}\langle\mathsf{Sen}(\mathsf{pp}, \mathsf{skey}, \mathsf{bag}, \mathsf{state}, \left[\!\left[\overrightarrow{\mathsf{val}}\right]\!\right], \mathsf{op}, \mathsf{val}), \mathsf{Rec}(\mathsf{pp}, \mathsf{rkey}, \mathsf{bag}, \left[\!\left[\overrightarrow{\mathsf{val}}\right]\!\right])\rangle$

- Sen retrieves a tag for the value from the map as $\mathsf{tag} \leftarrow \mathbb{B}[\overrightarrow{v}].\mathsf{Pop}()$, and computes commitments to this tag $((\llbracket \mathsf{tag} \rrbracket, \cdot), (\llbracket \mathsf{tag} \rrbracket)) \leftarrow \pi^{\mathsf{LCom}}_{\mathsf{Commit}}\langle\mathsf{Sen}(\mathsf{pp}, \mathsf{skey}, \mathsf{tag}), \mathsf{Rec}(\mathsf{pp}, \mathsf{rkey})\rangle$
- Sen and Rec add to the set of removed elements $\mathcal{R} \leftarrow \mathcal{R} \cup (\llbracket \mathsf{tag} \rrbracket \parallel \left[\!\left[\overrightarrow{\mathsf{val}}\right]\!\right])$

$((b), (b)) \leftarrow \pi^{\mathsf{ZKBag}}_{\mathsf{VerEmpty}}\langle\mathsf{Sen}(\mathsf{pp}, \mathsf{skey}, \mathsf{bag}, \mathsf{state}), \mathsf{Rec}(\mathsf{pp}, \mathsf{rkey}, \mathsf{bag})\rangle$

- Sen and Rec assert equality between the list of inserted and removed elements by invoking $\pi^{\mathsf{ZKMultiSet}}$ on $(\mathcal{I}, \mathcal{R})$

Figure 1: Public-coin "Interactive Zero-Knowledge Bag" sub-protocol implementing an interactive multi-set of secret values.

We give a concrete implementation of ZKBag in Figure 1. At a high level the protocol is as follows: during setup, the parties run the setup algorithm of the underlying linearly homomorphic commitment scheme (if there is one) π^{LCom} (see Section 3.1). During initialization, the parties just initialize three empty sets: (1) a set of committed values that were inserted into the bag $\mathcal{I}$, (2) a set of committed values that were removed from the bag $\mathcal{R}$, and (3) some private state $\mathbb{B}$ for the sender that will hold plaintext information about the committed values. Each time a (committed) item $\llbracket \overrightarrow{v} \rrbracket$ is inserted into the bag, the receiver samples a random $\mathsf{tag} \leftarrow\!\!\$\ \mathbb{F}$ and both parties add $(\llbracket \mathsf{tag} \rrbracket, \llbracket \overrightarrow{v} \rrbracket)$ to the set of "input elements" $\mathcal{I}$. Additionally, the sender records the tag and values by adding $(\mathsf{tag}, \overrightarrow{v})$ to $\mathbb{B}$. Whenever the sender wants to remove an element $\overrightarrow{v}$, they recall the appropriate tag using $\mathbb{B}$, creates a fresh commitment to $(\mathsf{tag}, \overrightarrow{v})$, and then both sides add the fresh commitment to the set of "removed elements" $\mathcal{R}$. The final check is simply checking (set) equality of the inserted and removed elements using the $\pi^{\mathsf{ZKMultiSet}} := (\pi^{\mathsf{ZKMultiSet}}_{\mathsf{Setup}}, \pi^{\mathsf{ZKMultiSet}}_{\mathsf{Prove}}, \pi^{\mathsf{ZKMultiSet}}_{\mathsf{Verify}})$ protocol

(see Section 3.5).

The intuition for why this simple protocol ensures that the sender cannot cheat by removing an element that was not previously inserted, is that the sender would need to guess the appropriate tag that will be sampled in the future, which they are only able to do with negligible probability $1/|\mathbb{F}|$. Therefore, they are restricted to "recalling" a previously inserted element, for which the tag is known. They are prevented from removing the element multiple times because the tags for each insertion should be unique (with high probability). $\pi^{\mathsf{ZKMultiSet}}$ ensures that insertion and removals are one-to-one. Formally, we prove the following theorem:

Theorem 4.1. *Assuming that π^{LCom} in a secure linearly homomorphic commitment scheme (see Section 3.1), and $\pi^{\mathsf{ZKMultiSet}}$ is a commit-and-prove style multi-set equality proof system (see Section 3.5), then π^{ZKBag}, shown in Figure 1, is a LinCom-Based Zero-Knowledge Bag, as defined in Definition 4.*

Correctness. By the correctness of $\Pi_{\mathsf{MultiSetEquality}}$, it is simple to see that Π_{ZKBag} is correct. Namely, if the pattern of insertions and removals is honest, ie. the insertions and removals are a permutation and each removal comes *after* its associated insertion, then Π_{ZKBag} will output 1 with high probability.

Knowledge Soundness. The extractor $\mathcal{E}$ runs by simply running the extractor of the linearly-homomorphic commitment scheme on each of $\{\mathsf{com}_i\}_{i\in[2n]}$. Denote the outputs of these extractors as $\mathsf{val}_1, \ldots, \mathsf{val}_{2n}$. Moreover, if Update_i is Remove, $\mathcal{E}$ runs the extractor of the linearly-homomorphic commitment scheme on the commitment to the tag created in that interaction. Denote the outputs of the extractors as $\mathsf{tag}_i^{\mathsf{Remove}}$. If any of these extractions fails, the extractors fails with error $\mathsf{Error}_{\mathsf{ComExtract}}$. Otherwise, $\mathcal{E}$ outputs $\mathsf{val}_1, \ldots, \mathsf{val}_{2n}$.

We now show that $\mathcal{E}$ will output a compliant set of values $\mathsf{val}_1, \ldots, \mathsf{val}_{2n}$ with high probability. Let NumInsert denote the number of insertions and NumRemove denote the number of insertions and removals in the interaction, respectively.

1. Note that the extractor only outputs $\mathsf{Error}_{\mathsf{ComExtract}}$ with $3n$ times the error rate of the extractor of the linearly-homomorphic commitment scheme, which, by the binding/extraction property of the linearly-homomorphic commitment scheme only happens with negligible probability.

2. Next, note that the probability of any two instances of Insert in the interaction sharing a value tag is $< \frac{n^2}{\mathbb{F}}$, as each tags was sampled uniformly at random from $\mathbb{F}$.

3. To fix notation, we create the following tuples for $i \in [2n]$:

   - If Update_i is Insert, then create the tuple $(i, \mathsf{tag}_i^{\mathsf{Insert}}, \mathsf{val}_i)$, where $\mathsf{tag}_i^{\mathsf{Insert}}$ is the tag generated during the execution of Update_i. Denote the set of all such tuples as $\{(\mathsf{timestamp}_j^{\mathsf{Insert}}, \mathsf{tag}_j^{\mathsf{Insert}}, \mathsf{val}_j^{\mathsf{Insert}})\}_{j\in[\mathsf{NumInsert}]}$
   - If Update_i is Remove, then create the tuple $(i, \mathsf{tag}_i^{\mathsf{Remove}}, \mathsf{val}_i)$, where $\mathsf{tag}_i^{\mathsf{Remove}}$ is the tag extracted above. Denote the set of all such tuples as $\{(\mathsf{timestamp}_j^{\mathsf{Remove}}, \mathsf{tag}_j^{\mathsf{Remove}}, \mathsf{val}_j^{\mathsf{Remove}})\}_{j\in[\mathsf{NumRemove}]}$

4. Next, note that by the soundness of the permutation check, $\mathsf{NumInsert} = \mathsf{NumRemove} = n$, and $\{(\mathsf{tag}_j^{\mathsf{Insert}}, \mathsf{val}_j^{\mathsf{Insert}})\}_{j\in[\mathsf{NumInsert}]}$ and $\{(\mathsf{tag}_j^{\mathsf{Remove}}, \mathsf{val}_j^{\mathsf{Remove}})\}_{j\in[\mathsf{NumRemove}]}$ are permutations of one another, except with negligible probability. Denote this permutation as f

5. Next, we observe that for each $(\mathsf{timestamp}_j^{\mathsf{Remove}}, \mathsf{tag}_j^{\mathsf{Remove}}, \mathsf{val}_j^{\mathsf{Remove}})$, there exists a $(\mathsf{timestamp}_{j'}^{\mathsf{Insert}}, \mathsf{tag}_{j'}^{\mathsf{Insert}}, \mathsf{val}_{j'}^{\mathsf{Insert}})$ with $\mathsf{timestamp}_{j'}^{\mathsf{Insert}} < \mathsf{timestamp}_j^{\mathsf{Remove}}$, except with probability $\frac{1}{|\mathbb{F}|}$. If this were not the case, then it would imply that the tag for the insertion must have been sampled after the removal and the prover must have correctly guessed a tag before it was sampled. Clearly this only happens with probability $\frac{1}{|\mathbb{F}|}$.

6. Finally, for each $(\mathsf{timestamp}_j^{\mathsf{Insert}}, \mathsf{tag}_j^{\mathsf{Insert}}, \mathsf{val}_j^{\mathsf{Insert}})$, with high probability there is a $(\mathsf{timestamp}_{j'}^{\mathsf{Remove}}, \mathsf{tag}_{j'}^{\mathsf{Remove}}, \mathsf{val}_{j'}^{\mathsf{Remove}})$ such that $\mathsf{timestamp}_{j'}^{\mathsf{Insert}} > \mathsf{timestamp}_j^{\mathsf{Remove}}$. This is true because the insertions and removals are permutations of one another, so for each insertions there must be a removal with the same tag. As before, if the timestamp of this insertion is not before the removal, then the prover must have guesses a tag before it was sampled, which only happens with probability $\frac{1}{|\mathbb{F}|}$.

We let the bijective map f be defined by a valid permutation between inserts and removals, which must exist with high probability, as described in (4). Note that this f is monotonically increasing by (5) and (6). Moreover, because we invoked the linearly homomorphic commitment scheme's extractor, for all computationally bounded adversaries $\mathcal{A}$ there is only a negligible probability that they could produce a valid equivocation to the commitments. Thus, with statistically small probability in the size of $\mathbb{F}$, the output of $\mathcal{E}$ is compliant with the definition.

Zero-knowledge. The simulator Sim simply follows the protocol executions described in Definition 4, and honestly follows the protocol at all steps. Note that the most significant difference is that the simulator commits to zero instead of other values, but otherwise the interactions are identical.

We now show that view of the receiver when interacting with the simulator is the computationally close to the view of the receiver interacting with the honest sender. We proceed with a hybrid argument. Let Hybrid_0 denote the interaction between the receiver and the honest sender.

- Hybrid_1 : Let Hybrid_1 be the same as Hybrid_0, but Sim simulates $\pi^{\mathsf{ZKMultiSet}}$ during $\pi^{\mathsf{ZKBag}}_{\mathsf{VerEmpty}}$. By the zero-knowledge property of $\pi^{\mathsf{ZKMultiSet}}$, the view of receiver in Hybrid_1 and Hybrid_0 are computationally close.
- $\mathsf{Hybrid}_2, \mathsf{Hybrid}_3, \ldots, \mathsf{Hybrid}_{2n+1}$: In each of these hybrids, instead of commiting to a real value, Sim commits to 0 instead. By the hiding property of the commitment scheme, the view of receiver in Hybrid_{i+1} and Hybrid_i are computationally close for $i \in [1, 2n+1]$.
- Hybrid_{2n+2} : Hybrid_{2n+2} is the same as Hybrid_{2n+1}, but Sim executes $\Pi_{\mathsf{MultiSetEquality}}$ honestly instead of simulating. Again, by the zero-knowledge property of $\Pi_{\mathsf{MultiSetEquality}}$, the view of receiver in Hybrid_{2n+1} and Hybrid_{2n+2} are computationally close.

Note that the view of the receiver in Hybrid_{2n+2} is distributed the same as the view of the receiver when interacting with the simulator above. Thus, we have concluded our proof.

5 Memory Consistency using ZKBag

When proving the correct execution of a RAM program, we need to ensure that memory is treated consistently. That is, each time an address is read from memory, only the value *last written* to that address is returned. Importantly, because we require zero-knowledge, this must be done without revealing executed programs memory access patterns. We observe that this matches perfectly with the property provided by ZKBag. Recall that memory can be seen as a sequence of tuples $(\mathsf{addr}, \mathsf{val})$, where addr is a unique address within the memory space and val is the current value being stored at that address. We can use ZKBag as a *key-value store* by dedicating the first part of the inserted value to be the key and the second part to be the value. That is, we store tuples of the form $(\mathsf{addr}, \mathsf{val})$ within the bag. The state of the bag corresponds to the "current" state of memory. Updating the contents of memory can be handled by updating the contents of the ZKBag.

Rather than give a formal definition for our protocol for handling memory π^{Memory}, we simply observe that the definitions are functionally equivalent to those for ZKBag, but the elements being inserted and removed from the bag now contain memory addresses. In order to make the semantics of our final construction easier to read, we provide a wrapper around the ZKBag with the names of common memory operations: Init, Read, Update, Verify:

- $((\mathsf{state}_\mathsf{P}), (\mathsf{state}_\mathsf{V})) \leftarrow \pi^{\mathsf{Memory}}_{\mathsf{Init}}$: The prover and verifier take in a set of public values that will make up the initial contents of memory. The result is some state held by both the sender and the receiver.
- $((\mathsf{state}_\mathsf{P}), (\mathsf{state}_\mathsf{V})) \leftarrow \pi^{\mathsf{Memory}}_{\mathsf{Update}}$: The prover and verifier each take in a commitment to the address and value that will be removed from memory $(\llbracket \mathsf{addr} \rrbracket, \llbracket \mathsf{val} \rrbracket)$ along with a commitment to the new value $\llbracket \mathsf{val}' \rrbracket$. Additionally, the prover takes in the actual value and opening to the commitments. The result is an updated state for both parties.
- $((\mathsf{state}_\mathsf{P}), (\mathsf{state}_\mathsf{V})) \leftarrow \pi^{\mathsf{Memory}}_{\mathsf{Read}}$: The prover and verifier each take in a commitment to the address and value that will be read from memory $(\llbracket \mathsf{addr} \rrbracket, \llbracket \mathsf{val} \rrbracket)$—or, more accurately, value that the prover *claims* will be the result of reading from the address. Additionally, the prover takes in the actual value and opening to the commitments. The result is an updated state for both parties.

$((\mathsf{state}_\mathsf{P}, \mathsf{state}_\mathsf{V}), (\mathsf{bag})) \leftarrow \pi^{\mathsf{Memory}}_{\mathsf{Init}}\langle \mathsf{P}(\{\mathsf{val}_{\mathsf{addr}}\}_{\mathsf{addr} \in 1\ldots,m}), \mathsf{V}(\{\mathsf{val}_{\mathsf{addr}}\}_{\mathsf{addr} \in 1\ldots,m})\rangle$

- P and V initialize and setup a ZKBag by invoking both $\pi^{\mathsf{ZKBag}}_{\mathsf{Setup}}$ and $\pi^{\mathsf{ZKBag}}_{\mathsf{Init}}$
- For each $\mathsf{addr} \in 1\ldots,m$:
  - P and V generate $[\![\mathsf{addr}]\!]$ and $[\![\mathsf{val}_{\mathsf{addr}}]\!]$ by invoking $\pi^{\mathsf{LCom}}_{\mathsf{Commit}}$ on shared randomness (to generate a public commitment).
  - P and V insert the tuple $([\![\mathsf{addr}]\!], [\![\mathsf{val}_{\mathsf{addr}}]\!])$ into the ZKBag by invoking $\pi^{\mathsf{ZKBag}}_{\mathsf{Insert}}$

$((\mathsf{bag}, \mathsf{state}), (\mathsf{bag})) \leftarrow \pi^{\mathsf{Memory}}_{\mathsf{Read}}\langle \mathsf{P}(\mathsf{state}_\mathsf{P}, ([\![\mathsf{addr}]\!], [\![\mathsf{val}]\!]), (\mathsf{op}_{\mathsf{addr}}, \mathsf{op}_{\mathsf{val}}), (\mathsf{addr}, \mathsf{val})), \mathsf{V}(\mathsf{state}_\mathsf{V}, ([\![\mathsf{addr}]\!], [\![\mathsf{val}]\!]))\rangle$

- P and V remove $([\![\mathsf{addr}]\!], [\![\mathsf{val}]\!])$ from the ZKBag by invoking $\pi^{\mathsf{ZKBag}}_{\mathsf{Remove}}$
- P and V insert $([\![\mathsf{addr}]\!], [\![\mathsf{val}]\!])$ into the ZKBag by invoking $\pi^{\mathsf{ZKBag}}_{\mathsf{Insert}}$

$((\mathsf{bag}, \mathsf{state}), (\mathsf{bag})) \leftarrow \pi^{\mathsf{Memory}}_{\mathsf{Update}}\langle \mathsf{P}(\mathsf{state}_\mathsf{P}, ([\![\mathsf{addr}]\!], [\![\mathsf{val}]\!], [\![\mathsf{val}']\!]), (\mathsf{op}_{\mathsf{addr}}, \mathsf{op}_{\mathsf{val}}, \mathsf{op}_{\mathsf{val}'}), (\mathsf{addr}, \mathsf{val}, \mathsf{val}')), \mathsf{V}(\mathsf{state}_\mathsf{V}, ([\![\mathsf{addr}]\!], [\![\mathsf{val}]\!], [\![\mathsf{val}']\!]))\rangle$

- P and V remove $([\![\mathsf{addr}]\!], [\![\mathsf{val}]\!])$ from the ZKBag by invoking $\pi^{\mathsf{ZKBag}}_{\mathsf{Remove}}$
- P and V insert $([\![\mathsf{addr}]\!], [\![\mathsf{val}']\!])$ into the ZKBag by invoking $\pi^{\mathsf{ZKBag}}_{\mathsf{Insert}}$

$((b), (b)) \leftarrow \pi^{\mathsf{Memory}}_{\mathsf{Verify}}\langle \mathsf{P}(\mathsf{state}_\mathsf{P}, \{\mathsf{val}_{\mathsf{addr}}\}_{\mathsf{addr} \in 1\ldots,m}), \mathsf{V}(\mathsf{state}_\mathsf{V}, \{\mathsf{val}_{\mathsf{addr}}\}_{\mathsf{addr} \in 1\ldots,m})\rangle$

- For each $\mathsf{addr} \in 1\ldots,m$:
  - P and V generate $[\![\mathsf{addr}]\!]$ and $[\![\mathsf{val}_{\mathsf{addr}}]\!]$ by invoking $\pi^{\mathsf{LCom}}_{\mathsf{Commit}}$ on shared randomness.
  - P and V remove the tuple $([\![\mathsf{addr}]\!], [\![\mathsf{val}_{\mathsf{addr}}]\!])$ from the ZKBag by invoking $\pi^{\mathsf{ZKBag}}_{\mathsf{Remove}}$.
- Finally, P and V check that ZKBag is empty by invoking $\pi^{\mathsf{ZKBag}}_{\mathsf{VerEmpty}}$

Figure 2: A memory-check protocol based on ZKbag.

- $((b), (b)) \leftarrow \pi^{\mathsf{Memory}}_{\mathsf{Verify}}$: The prover and verifier each take in their current state and a set of values (representing the current state of memory) and then output 1 if this is really the current state of memory and 0 otherwise. Optionally, the verifier can take any amount of these values in committed form (if they should remain private).

We provide a writeup of the memory checking protocol π^{Memory} in Figure 2. In brief, during $\pi^{\mathsf{Memory}}_{\mathsf{Init}}$, the parties initialize and setup the ZKBag, and then insert tuples with the address and values to the ZKBag. When invoking $\pi^{\mathsf{Memory}}_{\mathsf{Update}}$, the parties remove the old address-value tuple $([\![\mathsf{addr}]\!], [\![\mathsf{val}]\!])$ from the ZKBag and insert the new tuple $([\![\mathsf{addr}]\!], [\![\mathsf{val}']\!])$ into the ZKBag. Importantly, the commitment to the address $[\![\mathsf{addr}]\!]$ is consistent across the two protocol invocations. When invoking $\pi^{\mathsf{Memory}}_{\mathsf{Read}}$ the parties remove the address-value tuple $([\![\mathsf{addr}]\!], [\![\mathsf{val}]\!])$ and the reinsert the same tuple back into the ZKBag. Finally, when invoking $\pi^{\mathsf{Memory}}_{\mathsf{Verify}}$, the parties remove the remaining contents of the ZKBag and then call $\pi^{\mathsf{ZKBag}}_{\mathsf{VerEmpty}}$.

6 Verifying Processor Execution using ZKBag

When proving correct execution of a RAM program, the prover wants to convince the verifier that a "valid" instruction was executed at every step of the program. In particular, the verifier needs to be convinced that at each step, (1) the prover picked one of the instructions supported by the processor, (2) the picked instruction was executed honestly and (3) that the picked instruction is the "correct choice" based on the input dependent execution thus far. In this section, we present a new commit-and-prove style zero-knowledge protocol using ZKBag (see Section 4), that helps enforce the first two guarantees. Looking ahead, in the next section, we demonstrate how to combine this protocol with the protocol for memory consistency (see Section 5) to obtain a zero-knowledge proof system for RAM programs that enforces all of the above guarantees.

Disjunctive Relation $\mathcal{R}^{\mathsf{ZKDisj}}$. Our zero-knowledge protocol for checking correct execution of processor instructions, is a custom LinCom based commit-and-prove style zero-knowledge protocol (see Section 3.2) for the following relation: *Let $(\mathbf{A}_i, \mathbf{B}_i, \mathbf{C}_i)_{i\in[\ell]}$ be a set of ℓ R1CS instances. Given t commitments $(\llbracket \overrightarrow{\mathsf{z}_j} \rrbracket)_{j\in[t]}$ computed using $\pi^{\mathsf{LCom}}_{\mathsf{Commit}}$ (see Section 3.1), the prover/sender wants to convince the receiver/verifier that for each $j \in [t]$, it knows $\overrightarrow{\mathsf{z}_j}, \overrightarrow{\mathsf{op}_j}$ such that they form a valid opening for $\llbracket \mathsf{z}_j \rrbracket$ and an index $\alpha_j \in [\ell]$, such that $\overrightarrow{\mathsf{z}_j}$ is a valid extended witness for $(\mathbf{A}_{\alpha_j}, \mathbf{B}_{\alpha_j}, \mathbf{C}_{\alpha_j})$.*

Recall from Section 3.3, that for an R1CS relation, each extended witness is of the form $\overrightarrow{\mathsf{z}_j} = \overrightarrow{\mathsf{w}_j} \| \overrightarrow{\mathsf{x}_j} \| 1$, where $\overrightarrow{\mathsf{x}_j}$ is a part of the instance (which may or may not be known to the verifier), while $\overrightarrow{\mathsf{w}_j}$ is exclusively known only to the prover. Therefore, $\llbracket \overrightarrow{\mathsf{z}_j} \rrbracket$ can be parsed as $\llbracket \overrightarrow{\mathsf{w}_j} \rrbracket \| \llbracket \overrightarrow{\mathsf{x}_j} \rrbracket \| \llbracket 1 \rrbracket$. Here, we assume that $\llbracket \overrightarrow{\mathsf{w}_j} \rrbracket$ were computed using the "private-mode" (i.e., the default version) of a linearly homomorphic commitment scheme (Section 3.1), commitment $\llbracket 1 \rrbracket$ was computed in the "public-mode" (i.e., using shared randomness) and commitments $\llbracket \overrightarrow{\mathsf{x}_j} \rrbracket$ were computed in either the public-mode or the private-mode depending on whether or not $\overrightarrow{\mathsf{x}}$ is public to the verifier.

Commit-and-Prove ZK Proof System for $\mathcal{R}^{\mathsf{ZKDisj}}$. As discussed in Section 2.3, we design a commit-and-prove zero-knowledge proof system for $\mathcal{R}^{\mathsf{ZKDisj}}$ using a ZKBag protocol π^{ZKBag} (see Section 4) and the folding scheme for relaxed R1CS from [KST22]. Given these tools, our protocol is straightforward. The parties start by creating public commitments to trivially satisfied relaxed R1CS extended witnesses (i.e., just a vector of 0s) for each of the ℓ branches. They then initialize a ZKBag and store each of these commitments in the ZKbag (see Figure 1). We refer to these commitments as accumulators for the ℓ branches.Then for each step $j \in [t]$ of the processor, the parties proceed as follows: i) Parties retrieve the accumulator for the satisfied branch α_j from the ZKbag. ii) The prover computes cross terms $\overrightarrow{T}$ for the α_j^{th} branch using the retrieved accumulator and the new satisfied R1CS extended witness $\overrightarrow{\mathsf{z}_j}$ and computes a commitment to these cross terms. iii) The verifier samples a random field element. iv) The parties fold the retrieved accumulator onto the new satisfied R1CS extended witness $\overrightarrow{\mathsf{z}_j}$ using this random value. This forms the updated accumulator for the α_j^{th} branch. v) Store the updated accumulator in the bag. At the end, every accumulator is extracted from the bag, randomized and checked naively.

We note that a naïve strategy to design a commit-and-prove protocol for this relation without zero-knowledge would be to simply commit to the extended witness $\overrightarrow{\mathsf{z}_j}$ at each step, reveal the associated branch index α_j use any generic commit-and-prove proof system (e.g. QuickSilver [YSWW21]) to prove correct execution of this step. Our protocol achieves the *zero-knowledge* property while only incurring a multiplicative overhead of 4 of this naïve protocol. This is because our protocol requires committing to 4 vectors proportional to the length of $\overrightarrow{\mathsf{z}_j}$ and the ZKBag operations are independent of the dimension of the extended witness or R1CS relation. We include a formal description of this protocol in Figures 3 and 4.

$((\mathsf{pp}, \mathsf{skey}), (\mathsf{pp}, \mathsf{rkey})) \leftarrow \pi^{\mathsf{ZKDisj}}_{\mathsf{Setup}}\langle(\mathsf{Sen}(1^\lambda), \mathsf{Rec}(1^\lambda)\rangle$

- Sen and Rec invoke $((\mathsf{pp}^{\mathsf{LCom}}, \mathsf{skey}^{\mathsf{LCom}}), (\mathsf{pp}^{\mathsf{LCom}}, \mathsf{rkey}^{\mathsf{LCom}})) \leftarrow \pi^{\mathsf{LCom}}_{\mathsf{Setup}}\langle(\mathsf{Sen}(1^\lambda), \mathsf{Rec}(1^\lambda)\rangle$
- Output $(\mathsf{pp} = \mathsf{pp}^{\mathsf{LCom}}, \mathsf{skey} = \mathsf{skey}^{\mathsf{LCom}})$ to Sen and $(\mathsf{pp} = \mathsf{pp}^{\mathsf{LCom}}, \mathsf{rkey} = \mathsf{rkey}^{\mathsf{LCom}})$ to Rec.

$((\mathsf{Proof}^{\mathsf{ZK}}, \mathsf{st}), (\mathsf{Proof}^{\mathsf{ZK}})) \leftarrow \pi^{\mathsf{ZKDisj}}_{\mathsf{Prove}}\langle(\mathsf{Sen}(\mathsf{pp}, \mathsf{skey}, (\mathbf{A}_i, \mathbf{B}_i, \mathbf{C}_i)_{i\in[\ell]}, (\llbracket \overrightarrow{z_j} \rrbracket)_{j\in[t]}, (\overrightarrow{\mathsf{op}_{\mathsf{z}_j}})_{j\in[t]}, (\overrightarrow{z_j})_{j\in[t]}), \mathsf{Rec}(\mathsf{pp}, \mathsf{rkey}, (\mathbf{A}_i, \mathbf{B}_i, \mathbf{C}_i)_{i\in[\ell]}, (\llbracket \overrightarrow{z_j} \rrbracket)_{j\in[t]})\rangle$

---

1. **Initialization Phase:**
   - Sen and Rec initialize a ZKBag $((\mathsf{bag}_0, \mathsf{state}_0), (\mathsf{bag}_0)) \leftarrow \pi^{\mathsf{ZKBag}}_{\mathsf{Init}}\langle\mathsf{Sen}(\mathsf{pp}, \mathsf{skey}), \mathsf{Rec}(\mathsf{pp}, \mathsf{rkey})\rangle$.
   - For each $i \in [\ell]$, Sen and Rec invoke $((\llbracket \overrightarrow{\mathsf{z}_i^0} \rrbracket, \mathsf{op}_{\mathsf{z}_i^0}), (\llbracket \overrightarrow{\mathsf{z}_i^0} \rrbracket)) \leftarrow \pi^{\mathsf{LCom}}_{\mathsf{Commit}}\langle\mathsf{Sen}(\mathsf{pp}, \mathsf{skey}, \overrightarrow{0}), \mathsf{Rec}(\mathsf{pp}, \mathsf{rkey})\rangle$ and $((\llbracket \overrightarrow{\mathsf{e}_i^0} \rrbracket, \mathsf{op}_{\mathsf{e}_i^0}), (\llbracket \overrightarrow{\mathsf{e}_i^0} \rrbracket)) \leftarrow \pi^{\mathsf{LCom}}_{\mathsf{Commit}}\langle\mathsf{Sen}(\mathsf{pp}, \mathsf{skey}, \overrightarrow{0}), \mathsf{Rec}(\mathsf{pp}, \mathsf{rkey}, \overrightarrow{0})\rangle$ on shared randomness, to compute public commitments to a trivially satisfied relaxed-R1CS instance and stores them in the ZKBag

$$((\mathsf{bag}_{2i-1}, \mathsf{state}_{2i-1}), (\mathsf{bag}_{2i-1})) \leftarrow \pi^{\mathsf{ZKBag}}_{\mathsf{Insert}}\langle\mathsf{Sen}(\mathsf{pp}, \mathsf{skey}, \mathsf{bag}_{2i-2}, \mathsf{state}_{2i-2}, \llbracket \overrightarrow{\mathsf{z}_i^0} \rrbracket, \mathsf{op}_{\mathsf{z}_i^0}, \overrightarrow{\mathsf{z}_i^0}), \mathsf{Rec}(\mathsf{pp}, \mathsf{rkey}, \mathsf{bag}_{2i-2}, \llbracket \overrightarrow{\mathsf{z}_i^0} \rrbracket)\rangle$$

$$((\mathsf{bag}_{2i}, \mathsf{state}_{2i}), (\mathsf{bag}_{2i})) \leftarrow \pi^{\mathsf{ZKBag}}_{\mathsf{Insert}}\langle\mathsf{Sen}(\mathsf{pp}, \mathsf{skey}, \mathsf{bag}_{2i-1}, \mathsf{state}_{2i-1}, \llbracket \overrightarrow{\mathsf{e}_i^0} \rrbracket, \mathsf{op}_{\mathsf{e}_i^0}, \overrightarrow{\mathsf{e}_i^0}), \mathsf{Rec}(\mathsf{pp}, \mathsf{rkey}, \mathsf{bag}_{2i-1}, \llbracket \overrightarrow{\mathsf{e}_i^0} \rrbracket)\rangle$$

   - Sen initializes a local map $\mathbb{M}$ maintaining the state of each of the ℓ accumulators: $\forall i \in [\ell],\ \mathbb{M}[i] \leftarrow (\overrightarrow{\mathsf{z}_i}, \overrightarrow{\mathsf{e}_i})$.
2. **Execution Phase:** For each $j \in [t]$,
   - Given as input an index $\alpha_j \in [\ell]$, Sen retrieves the state of the α_j'th accumulator $(\overrightarrow{\mathsf{z}}', \overrightarrow{\mathsf{e}}') \leftarrow \mathbb{M}[\alpha_j]$, computes the cross terms

$$\overrightarrow{T} = \mathbf{A} \cdot \overrightarrow{z}' \circ \mathbf{B} \cdot \overrightarrow{z_j} + \mathbf{A} \cdot \overrightarrow{z_j} \circ \mathbf{B} \cdot \overrightarrow{z}' - \mathsf{u}_1 \cdot \mathbf{C} \cdot \overrightarrow{z_j} - \mathsf{u}_2 \cdot \mathbf{C} \cdot \overrightarrow{z}'$$

   - Sen and Rec invoke the following to compute commitments to the retrieved accumulator and these cross terms

$$((\llbracket \overrightarrow{\mathsf{z}'} \rrbracket, \mathsf{op}_{\mathsf{z}'}), (\llbracket \overrightarrow{\mathsf{z}'} \rrbracket)) \leftarrow \pi^{\mathsf{LCom}}_{\mathsf{Commit}}\langle\mathsf{Sen}(\mathsf{pp}, \mathsf{skey}, \overrightarrow{\mathsf{z}'}), \mathsf{Rec}(\mathsf{pp}, \mathsf{rkey})\rangle, \quad ((\llbracket \overrightarrow{\mathsf{e}'} \rrbracket, \mathsf{op}_{\mathsf{e}'}), (\llbracket \overrightarrow{\mathsf{e}'} \rrbracket)) \leftarrow \pi^{\mathsf{LCom}}_{\mathsf{Commit}}\langle\mathsf{Sen}(\mathsf{pp}, \mathsf{skey}, \overrightarrow{\mathsf{e}'}), \mathsf{Rec}(\mathsf{pp}, \mathsf{rkey})\rangle$$

$$((\llbracket \overrightarrow{T} \rrbracket, \mathsf{op}_T), (\llbracket \overrightarrow{T} \rrbracket)) \leftarrow \pi^{\mathsf{LCom}}_{\mathsf{Commit}}\langle\mathsf{Sen}(\mathsf{pp}, \mathsf{skey}, \overrightarrow{T}), \mathsf{Rec}(\mathsf{pp}, \mathsf{rkey})\rangle$$

   - Sen and Rec remove the old accumulator corresponding to the α_j'th index from the ZKBag. To simplify the notation, let $\rho = 2\ell + 4j - 2$.

$$((\mathsf{bag}_{\rho-1}, \mathsf{state}_{\rho-1}), (\mathsf{bag}_{\rho-1})) \leftarrow \pi^{\mathsf{ZKBag}}_{\mathsf{Remove}}\langle\mathsf{Sen}(\mathsf{pp}, \mathsf{skey}, \mathsf{bag}_{\rho-2}, \mathsf{state}_{\rho-2}, \llbracket \overrightarrow{\mathsf{z}'} \rrbracket, \mathsf{op}_{\mathsf{z}'}, \overrightarrow{\mathsf{z}'}), \mathsf{Rec}(\mathsf{pp}, \mathsf{rkey}, \mathsf{bag}_{\rho-2}, \llbracket \overrightarrow{\mathsf{z}'} \rrbracket)\rangle$$

$$((\mathsf{bag}_{\rho}, \mathsf{state}_{\rho}), (\mathsf{bag}_{\rho})) \leftarrow \pi^{\mathsf{ZKBag}}_{\mathsf{Remove}}\langle\mathsf{Sen}(\mathsf{pp}, \mathsf{skey}, \mathsf{bag}_{\rho-1}, \mathsf{state}_{\rho-1}, \llbracket \overrightarrow{\mathsf{e}'} \rrbracket, \mathsf{op}_{\mathsf{e}'}, \overrightarrow{\mathsf{e}'}), \mathsf{Rec}(\mathsf{pp}, \mathsf{rkey}, \mathsf{bag}_{\rho-1}, \llbracket \overrightarrow{\mathsf{e}'} \rrbracket)\rangle$$

   - Rec samples a random $r \leftarrow\$ \mathbb{F}$ and sends it to Sen.
   - Sen and Rec update the α_j'th accumulator

$$\llbracket \overrightarrow{\mathsf{e}} \rrbracket \leftarrow \llbracket \overrightarrow{\mathsf{e}}' \rrbracket + r \cdot \llbracket \overrightarrow{T} \rrbracket \qquad \llbracket \overrightarrow{\mathsf{z}} \rrbracket \leftarrow \llbracket \overrightarrow{\mathsf{z}}' \rrbracket + r \cdot \llbracket \overrightarrow{\mathsf{z}}_j \rrbracket$$

     and insert the updated accumulator in ZKBag. As before, let $\rho = 2\ell + 4j - 2$.

$$((\mathsf{bag}_{\rho+1}, \mathsf{state}_{\rho+1}), (\mathsf{bag}_{\rho+1})) \leftarrow \pi^{\mathsf{ZKBag}}_{\mathsf{Insert}}\langle\mathsf{Sen}(\mathsf{pp}, \mathsf{skey}, \mathsf{bag}_{\rho}, \mathsf{state}_{\rho}, \llbracket \overrightarrow{\mathsf{z}} \rrbracket, \mathsf{op}_{\mathsf{z}}, \overrightarrow{\mathsf{z}}), \mathsf{Rec}(\mathsf{pp}, \mathsf{rkey}, \mathsf{bag}_{\rho-1}, \llbracket \overrightarrow{\mathsf{z}} \rrbracket)\rangle$$

$$((\mathsf{bag}_{\rho+2}, \mathsf{state}_{\rho+2}), (\mathsf{bag}_{\rho+2})) \leftarrow \pi^{\mathsf{ZKBag}}_{\mathsf{Insert}}\langle\mathsf{Sen}(\mathsf{pp}, \mathsf{skey}, \mathsf{bag}_{\rho+1}, \mathsf{state}_{\rho+1}, \llbracket \overrightarrow{\mathsf{e}} \rrbracket, \mathsf{op}_{\mathsf{e}}, \overrightarrow{\mathsf{e}}), \mathsf{Rec}(\mathsf{pp}, \mathsf{rkey}, \mathsf{bag}_{\rho+1}, \llbracket \overrightarrow{\mathsf{e}} \rrbracket)\rangle$$

Figure 3: Part 1 of zero-knowledge protocol for checking processor instructions.

$((b),(b)) \leftarrow \pi^{\mathsf{ZKDisj}}_{\mathsf{Verify}}\langle \mathsf{Sen}(\mathsf{pp},\mathsf{skey},\mathsf{Proof}^{\mathsf{ZK}},\mathsf{st},(\mathbf{A}_i,\mathbf{B}_i,\mathbf{C}_i)_{i\in[\ell]}), \mathsf{Rec}(\mathsf{pp},\mathsf{rkey},\mathsf{Proof}^{\mathsf{ZK}},(\mathbf{A}_i,\mathbf{B}_i,\mathbf{C}_i)_{i\in[\ell]})\rangle$

- Sen proceeds as follows for each $i \in [\ell]$
  1. Generate random relaxed R1CS instance $\mathsf{z}_{(i,2)} \leftarrow\$ \mathbb{F}^m$, where $\overrightarrow{\mathsf{z}_{(i,2)}} = \overrightarrow{\mathsf{w}_{(i,2)}} \| \overrightarrow{\mathsf{x}_{(i,2)}} \| \overrightarrow{\mathsf{u}_{(i,2)}}$.
  2. Compute the corresponding error term
  $$\overrightarrow{L} \leftarrow (\mathbf{A}_i \cdot \overrightarrow{\mathsf{z}_{(i,2)}}) \circ (\mathbf{B}_i \cdot \overrightarrow{\mathsf{z}_{(i,2)}}) \qquad \overrightarrow{R} \leftarrow \mathsf{u}_{(i,2)} \cdot (\mathbf{C}_i \cdot \overrightarrow{\mathsf{z}_{(i,2)}}) \qquad \overrightarrow{\mathsf{e}_{(i,2)}} \leftarrow \overrightarrow{L} - \overrightarrow{R}$$
  3. Retrieve the i'th accumulator state $(\overrightarrow{\mathsf{z}_{(i,1)}}, \overrightarrow{\mathsf{e}_{(i,1)}}) \leftarrow \mathbb{M}[i]$ and compute cross terms as
  $$\overrightarrow{\delta_1} \leftarrow \mathbf{A}_i \cdot \overrightarrow{\mathsf{z}_{(i,1)}} \circ \mathbf{B}_i \cdot \overrightarrow{\mathsf{z}_{(i,2)}} \quad \overrightarrow{\delta_2} \leftarrow \mathbf{A}_i \cdot \overrightarrow{\mathsf{z}_{(i,2)}} \circ \mathbf{B}_i \cdot \overrightarrow{\mathsf{z}_{(i,1)}} \quad \overrightarrow{\delta_3} \leftarrow \mathsf{u}_{(i,1)} \cdot \mathbf{C}_i \cdot \overrightarrow{\mathsf{z}_{(i,2)}} \quad \overrightarrow{\delta_4} \leftarrow \mathsf{u}_{(i,2)} \cdot \mathbf{C}_i \cdot \overrightarrow{\mathsf{z}_{(i,1)}}$$
  $$\overrightarrow{T_i} \leftarrow \overrightarrow{\delta_1} + \overrightarrow{\delta_2} - \overrightarrow{\delta_3} - \overrightarrow{\delta_4}$$
  4. Computes commitments to the two accumulators and the cross terms
  $$((\llbracket \overrightarrow{T_i} \rrbracket, \mathsf{op}_{T_i}), (\llbracket \overrightarrow{T_i} \rrbracket)) \leftarrow \pi^{\mathsf{LCom}}_{\mathsf{Commit}}\langle \mathsf{Sen}(\mathsf{pp},\mathsf{skey},\overrightarrow{T_i}), \mathsf{Rec}(\mathsf{pp},\mathsf{rkey})\rangle$$
  $$((\llbracket \overrightarrow{\mathsf{z}_{(i,1)}} \rrbracket, \mathsf{op}_{\mathsf{z}_{(i,1)}}), (\llbracket \overrightarrow{\mathsf{z}_{(i,1)}} \rrbracket)) \leftarrow \pi^{\mathsf{LCom}}_{\mathsf{Commit}}\langle \mathsf{Sen}(\mathsf{pp},\mathsf{skey},\overrightarrow{\mathsf{z}_{(i,1)}}), \mathsf{Rec}(\mathsf{pp},\mathsf{rkey})\rangle, \quad ((\llbracket \overrightarrow{\mathsf{z}_{(i,2)}} \rrbracket, \mathsf{op}_{\mathsf{z}_{(i,2)}}), (\llbracket \overrightarrow{\mathsf{z}_{(i,2)}} \rrbracket)) \leftarrow \pi^{\mathsf{LCom}}_{\mathsf{Commit}}\langle \mathsf{Sen}(\mathsf{pp},\mathsf{skey},\overrightarrow{\mathsf{z}_{(i,2)}}), \mathsf{Rec}(\mathsf{pp},\mathsf{rkey})\rangle$$
  $$((\llbracket \overrightarrow{\mathsf{e}_{(i,1)}} \rrbracket, \mathsf{op}_{\mathsf{e}_{(i,1)}}), (\llbracket \overrightarrow{\mathsf{e}_{(i,1)}} \rrbracket)) \leftarrow \pi^{\mathsf{LCom}}_{\mathsf{Commit}}\langle \mathsf{Sen}(\mathsf{pp},\mathsf{skey},\overrightarrow{\mathsf{e}_{(i,1)}}), \mathsf{Rec}(\mathsf{pp},\mathsf{rkey})\rangle, \quad ((\llbracket \overrightarrow{\mathsf{e}_{(i,2)}} \rrbracket, \mathsf{op}_{\mathsf{e}_{(i,2)}}), (\llbracket \overrightarrow{\mathsf{e}_{(i,2)}} \rrbracket)) \leftarrow \pi^{\mathsf{LCom}}_{\mathsf{Commit}}\langle \mathsf{Sen}(\mathsf{pp},\mathsf{skey},\overrightarrow{\mathsf{e}_{(i,2)}}), \mathsf{Rec}(\mathsf{pp},\mathsf{rkey})\rangle$$

- Rec samples a random $r \leftarrow\$ \mathbb{F}$ and sends it to Sen.
- For each $i \in [\ell]$, Sen and Rec proceed as follows:
  1. Remove the i'th accumulator from ZKBag. To simplify notation, let $\tau = 2\ell + 4t + 2i$.
  $$((\mathsf{bag}_{\tau-1},\mathsf{state}_{\tau-1}),(\mathsf{bag}_{\tau-1})) \leftarrow \pi^{\mathsf{ZKBag}}_{\mathsf{Remove}}\langle \mathsf{Sen}(\mathsf{pp},\mathsf{skey},\mathsf{bag}_{\tau-2},\mathsf{state}_{\tau-2},\llbracket \overrightarrow{\mathsf{z}_{(i,1)}} \rrbracket, \mathsf{op}_{\mathsf{z}_i},\overrightarrow{\mathsf{z}_i}), \mathsf{Rec}(\mathsf{pp},\mathsf{rkey},\mathsf{bag}_{\tau-2},\llbracket \overrightarrow{\mathsf{z}_{(i,1)}} \rrbracket)\rangle$$
  $$((\mathsf{bag}_{\tau},\mathsf{state}_{\tau}),(\mathsf{bag}_{\tau})) \leftarrow \pi^{\mathsf{ZKBag}}_{\mathsf{Remove}}\langle \mathsf{Sen}(\mathsf{pp},\mathsf{skey},\mathsf{bag}_{\tau-1},\mathsf{state}_{\tau-1},\llbracket \overrightarrow{\mathsf{e}_{(i,1)}} \rrbracket, \mathsf{op}_{\mathsf{e}_i},\overrightarrow{\mathsf{e}_i}), \mathsf{Rec}(\mathsf{pp},\mathsf{rkey},\mathsf{bag}_{\tau-1},\llbracket \overrightarrow{\mathsf{e}_{(i,1)}} \rrbracket)\rangle$$
  2. Accumulate with the blinding instance
  $$\llbracket \overrightarrow{\mathsf{e}_i} \rrbracket \leftarrow \llbracket \overrightarrow{\mathsf{e}_{(i,1)}} \rrbracket + r \cdot \llbracket \overrightarrow{T_i} \rrbracket + r^2 \cdot \llbracket \overrightarrow{\mathsf{e}_{(i,2)}} \rrbracket \qquad \llbracket \overrightarrow{\mathsf{z}_i} \rrbracket \leftarrow \llbracket \overrightarrow{\mathsf{z}_{(i,1)}} \rrbracket + r \cdot \llbracket \overrightarrow{\mathsf{z}_{(i,2)}} \rrbracket \qquad \mathsf{u}_i = \mathsf{u}_{(i,1)} + r \cdot \mathsf{u}_{(i,2)}$$

- They check whether the ZKBag is empty $((1),(1)) \leftarrow \pi^{\mathsf{ZKBag}}_{\mathsf{VerEmpty}}\langle \mathsf{Sen}(\mathsf{pp},\mathsf{skey},\mathsf{bag}_{4\ell+4j},\mathsf{state}_{4\ell+4j}), \mathsf{Rec}(\mathsf{pp},\mathsf{rkey},\mathsf{bag}_{4\ell+4j})\rangle$.
- For each $i \in [\ell]$, Sen opens the following commitments to Rec
$$((1),(\overrightarrow{\mathsf{e}_i})) \leftarrow \pi^{\mathsf{LCom}}_{\mathsf{Open}}\langle \mathsf{Sen}(\mathsf{pp},\mathsf{skey},\llbracket \overrightarrow{\mathsf{e}_i} \rrbracket, \mathsf{op}_{\overrightarrow{\mathsf{e}_i}},\overrightarrow{\mathsf{e}_i}), \mathsf{Rec}(\mathsf{pp},\mathsf{rkey},\llbracket \overrightarrow{\mathsf{e}_i} \rrbracket)\rangle$$
$$((1),(\overrightarrow{\mathsf{z}_i})) \leftarrow \pi^{\mathsf{LCom}}_{\mathsf{Open}}\langle \mathsf{Sen}(\mathsf{pp},\mathsf{skey},\llbracket \overrightarrow{\mathsf{z}_i} \rrbracket, \mathsf{op}_{\overrightarrow{\mathsf{z}_i}},\overrightarrow{\mathsf{z}_i}), \mathsf{Rec}(\mathsf{pp},\mathsf{rkey},\llbracket \overrightarrow{\mathsf{z}_i} \rrbracket)\rangle$$
- Finally, for each $i \in [\ell]$, Rec verifies the extended witness
$$\mathbf{A}_i \cdot \overrightarrow{\mathsf{z}_i} \circ \mathbf{B}_i \cdot \overrightarrow{\mathsf{z}_i} \stackrel{?}{=} \mathsf{u}_i \cdot (\mathbf{C} \cdot \overrightarrow{\mathsf{z}_i}) + \mathsf{e}_i$$

Figure 4: Part 2 of zero-knowledge protocol for checking processor instructions.

Theorem 6.1. *Assuming that π^{LCom} in a secure linearly homomorphic commitment scheme (see Section 3.1), and π^{ZKBag} is a zero-knowledge bag (see Section 4), then π^{ZKDisj}, shown in Figures 3 and 4, is a LinCom-based commit-and-prove zero-knowledge as defined in Section 3.2 for $\mathcal{R}^{\mathsf{ZKBag}}$.*

Proof. **Correctness.** Correctness follows from correctness of Linearly Homomorphic commitment, ZKBag and the folding property of relaxed R1CS (see Section 3.3).

Zero-Knowledge. Let $\mathsf{Sim}^{\mathsf{ZKBag}} = (\mathsf{Sim}^{\mathsf{ZKBag}}_{\mathsf{Setup}}, \mathsf{Sim}^{\mathsf{ZKBag}}_{\mathsf{Init}}, \mathsf{Sim}^{\mathsf{ZKBag}}_{\mathsf{Insert}}, \mathsf{Sim}^{\mathsf{ZKBag}}_{\mathsf{Remove}}, \mathsf{Sim}^{\mathsf{ZKBag}}_{\mathsf{VerEmpty}})$ be the simulator for ZKBag. We now describe the simulator Sim for our π^{ZKDisj} protocol.

1. *Setup:* Sim uses $\mathsf{Sim}^{\mathsf{ZKBag}}_{\mathsf{Setup}}$ to simulate the setup protocol.

2. *Initialization Phase:* Sim uses $\mathsf{Sim}^{\mathsf{ZKBag}}_{\mathsf{Init}}$ to simulate initializing a ZKBag. For each $i \in [\ell]$, it then honestly invokes $\pi^{\mathsf{LCom}}_{\mathsf{Commit}}$ to compute public commitments to trivially satisfied relaxed-R1CS instances and uses $\mathsf{Sim}^{\mathsf{ZKBag}}_{\mathsf{Insert}}$ to simulate inserting thses commitments in the simulated ZKBag. Sim also initializes the map $\mathbb{M}$ as described in the protocol.

3. *Execution Phase:* For each $j \in [t]$, Sim proceeds as follows: Set $\overrightarrow{\mathsf{w}_j} = \overrightarrow{0}$. Additioanlly, if $\overrightarrow{\mathsf{x}_j}$ is unknown to the receiver, set $\overrightarrow{\mathsf{x}_j} = \overrightarrow{0}$. Invoke $\pi^{\mathsf{LCom}}_{\mathsf{Commit}}$ to compute a commitment to $\overrightarrow{\mathsf{z}_j} = \overrightarrow{\mathsf{x}_j} \| \overrightarrow{\mathsf{w}_j} \| 1$. Set $\overrightarrow{\mathsf{z}'} = \overrightarrow{\mathsf{e}'} = \overrightarrow{T} = \overrightarrow{0}$. It honestly invokes $\pi^{\mathsf{LCom}}_{\mathsf{Commit}}$ to compute commitments to these values. Use $\mathsf{Sim}^{\mathsf{ZKBag}}_{\mathsf{Remove}}$ to simulate removing $[\![\overrightarrow{\mathsf{z}'}]\!]$ and $[\![\overrightarrow{\mathsf{e}'}]\!]$ from the simulated bag. Finally, it samples $r \leftarrow\!\$\, \mathbb{F}$, computes $[\![\overrightarrow{\mathsf{z}}]\!]$ and $[\![\overrightarrow{\mathsf{e}}]\!]$ using r and the above commitments as described in the protocol using $\pi^{\mathsf{LCom}}_{\mathsf{Comb}}$. Finally, it uses $\mathsf{Sim}^{\mathsf{ZKBag}}_{\mathsf{Insert}}$ to simulate inserting $[\![\overrightarrow{\mathsf{z}}]\!]$ and $[\![\overrightarrow{\mathsf{e}}]\!]$ in the simulated ZKBag.

4. *Verification Protocol:* For each $i \in [\ell]$, the simulator sets $\overrightarrow{T_i} = \overrightarrow{\mathsf{z}_{(i,1)}} = \overrightarrow{\mathsf{z}_{(i,2)}} = \overrightarrow{\mathsf{e}_{(i,1)}} = \overrightarrow{\mathsf{e}_{(i,2)}} = \overrightarrow{0}$ and invokes $\pi^{\mathsf{LCom}}_{\mathsf{Commit}}$ to compute commitments to these values. For each $i \in [\ell]$, it then samples $r \leftarrow\!\$\, \mathbb{F}$ and uses $\mathsf{Sim}^{\mathsf{ZKBag}}_{\mathsf{Remove}}$ to simulate removing $[\![\overrightarrow{\mathsf{z}_i}]\!]$ and $[\![\overrightarrow{\mathsf{e}_i}]\!]$ from the simulated ZKBag. Uses the above commitments along with r to compute $[\![\overrightarrow{\mathsf{z}_i}]\!]$ and $[\![\overrightarrow{\mathsf{e}_i}]\!]$ as described in the protocol using $\pi^{\mathsf{LCom}}_{\mathsf{Comb}}$. Then use $\mathsf{Sim}^{\mathsf{ZKBag}}_{\mathsf{VerEmpty}}$ to simulate demonstrating that the ZKBag is empty. Finally, for each $i \in [\ell]$, it samples $\overrightarrow{\mathsf{z}_i}, \overrightarrow{\mathsf{e}_i}$ such that $\mathbf{A}_i \cdot \overrightarrow{\mathsf{z}_i} \circ \mathbf{B}_i \cdot \overrightarrow{\mathsf{z}_i} =^{?} = \mathsf{u}_i \cdot (\mathbf{C} \cdot \overrightarrow{\mathsf{z}_i}) + \mathsf{e}_i$. It uses these values and runs $\mathsf{Equiv}^{\mathsf{LCom}}$ to compute an equivocal opening for $\overrightarrow{\mathsf{z}_i}, \overrightarrow{\mathsf{e}_i}$ and invokes $\pi^{\mathsf{LCom}}_{\mathsf{Open}}$ using these openings.

We now show that view of the receiver when interacting with the simulator Sim is the computationally close to the view of the receiver interacting with the honest sender. We proceed with a hybrid argument. Let Hybrid_0 denote the interaction between the receiver and the honest sender.

- Hybrid_1 : Let Hybrid_1 be the same as Hybrid_0, but Sim simulates π^{ZKBag}. By the zero-knowledge property of π^{ZKBag}, the view of the receiver in Hybrid_1 and Hybrid_0 are computationally close.
- Hybrid_2 : This hybrid is similar to Hybrid_1, except that in the verification protocol in this hybrid, for each $i \in [\ell]$, Sim samples $\overrightarrow{\mathsf{z}_i}, \overrightarrow{\mathsf{e}_i}$ such that $\mathbf{A}_i \cdot \overrightarrow{\mathsf{z}_i} \circ \mathbf{B}_i \cdot \overrightarrow{\mathsf{z}_i} =^{?} = \mathsf{u}_i \cdot (\mathbf{C} \cdot \overrightarrow{\mathsf{z}_i}) + \mathsf{e}_i$. It uses these values and runs $\mathsf{Equiv}^{\mathsf{LCom}}$ to compute an equivocal opening for $\overrightarrow{\mathsf{z}_i}, \overrightarrow{\mathsf{e}_i}$ and invokes $\pi^{\mathsf{LCom}}_{\mathsf{Open}}$ using these openings. By equivocation property π^{LCom}, the view of the receiver in Hybrid_1 and Hybrid_2 are computationally close.
- Hybrid_3 This hybrid is the same as Hybrid_2, except that instead of computing commitments to honestly computed values, Sim computes commitments to $\overrightarrow{0}$. By the hiding property of π^{LCom}, view of receiver in Hybrid_2 and Hybrid_3 are computationally close.

Note that the view of the receiver in Hybrid_3 is distributed the same as the view of the receiver when interacting with the simulator above. Thus, we have concluded our proof.

Knowledge Soundness. Let $\mathcal{E}^{\mathsf{LCom}}$ be the extractor of the linearly homomorphic commitment scheme. Given a verifying proof transcript for π^{ZKDisj}, the extractor $\mathcal{E}$ for our π^{ZKDisj} protocol runs $\mathcal{E}^{\mathsf{LCom}}$ to simply extract the extended witness $\overrightarrow{\mathsf{z}_j}$ from $[\![\overrightarrow{\mathsf{z}_j}]\!]$, for each $j \in [t]$. The probability that the $\exists j^* \in [t]$, such that for each $i \in [\ell]$, the extracted $\overrightarrow{\mathsf{z}_j}$ is not a satisfying extended witness for $(\mathbf{A}_i, \mathbf{B}_i, \mathbf{C}_i)$ depends on the following:

- $\mathcal{E}^{\mathsf{LCom}}$ failed to extract the correct value, which only happens with negligible probability due to the binding property of π^{LCom}.
- The adversary succeeds in violating knowledge soundness of π^{ZKBag}, which also happens with negligible probability.
- The adversary manages to cheat by successfully guessing at least one of the $t + \ell$ random challenges sampled by the verifier. Since the verifier samples these challenges uniformly at random from $\mathbb{F}$, this probability is $\frac{t+\ell}{/}|\mathbb{F}|$, which is exponentially small for a large field.

Therefore, the overall probability that this extractor fails to extract a satisfying set of extended witnesses from a verifying transcript is negligbly small. □

7 Dora: Zero-Knowledge for RAM Programs

In this section, we show how to compose the memory consistency protocol from Section 5 and our protocol for checking processor instructions from Section 6 to realize a zero-knowledge proof system for RAM programs.

RAM Program (Von Neumann Architecture). At each step, the processor maintains a local state $\overrightarrow{\mathsf{st}} = (\mathsf{pc}, \mathsf{Reg}_1, \ldots, \mathsf{Reg}_k)$, where pc denotes the program counter and we use $\mathsf{Reg}_1, \ldots, \mathsf{Reg}_k$ to refer to values stored in its local registers. Let $\mathcal{I} = \{I_1, \ldots, I_\ell\}$ be the set instructions supported by the processor.

NP Relation $\mathcal{R}^{\mathsf{zkRAM}}$. In order to prove correct execution of a RAM program, we design a custom LinCom based commit-and-prove style zero-knowledge proof system (see 3.2) for the following relation: *Let $\overrightarrow{M_0}$ denote the public initial state of the memory and $\overrightarrow{\mathsf{st}_0}$ denote the initial state of the processor (which is not public). For each processor step $j \in [t]$, given commitments $\left[\!\left[\overrightarrow{\mathsf{st}_j}\right]\!\right]$, $[\![\mathsf{inst}_j]\!]$, $\left[\!\left[\overrightarrow{\mathsf{ReadVal}_j}\right]\!\right]$, $\left[\!\left[\overrightarrow{\mathsf{OldWriteVal}_j}\right]\!\right]$, where $\left[\!\left[\overrightarrow{\mathsf{st}_j}\right]\!\right]$ is a concatenation of commitments to the program counter $\left[\!\left[\overrightarrow{\mathsf{pc}_j}\right]\!\right]$ and values stored in the registers including (but not limited to) $\left[\!\left[\overrightarrow{\mathsf{ReadAddr}_j}\right]\!\right]$, $\left[\!\left[\overrightarrow{\mathsf{WriteAddr}_j}\right]\!\right]$, $\left[\!\left[\overrightarrow{\mathsf{WriteVal}_j}\right]\!\right]$, the prover wants to convince the verifier that it knows the corresponding values and opening information such that the following is satisfied:*

- inst_j *is the value stored in the memory at location* $\overrightarrow{\mathsf{pc}_{j-1}}$.
- $\overrightarrow{\mathsf{ReadAddr}_j}$ *is stored in the appropriate registers in* $\overrightarrow{\mathsf{st}_{j-1}}$ *and* $\overrightarrow{\mathsf{ReadVal}_j}$ *is the value stored in the memory at location* $\overrightarrow{\mathsf{ReadAddr}_j}$.
- $\overrightarrow{\mathsf{st}_j}$ *(containing* $\overrightarrow{\mathsf{WriteAddr}_j}$, $\overrightarrow{\mathsf{WriteVal}_j}$ *in the appropriate registers) is the outcome of evaluating* I_{inst_j} *on input* $\overrightarrow{\mathsf{st}_{j-1}}$, $\overrightarrow{\mathsf{ReadVal}_j}$.
- *Old value* $\overrightarrow{\mathsf{OldWriteVal}_j}$ *at location* $\overrightarrow{\mathsf{WriteAddr}_j}$ *in the memory is replaced with* $\overrightarrow{\mathsf{WriteVal}_j}$.

For each $i \in [\ell]$, we use $(\mathbf{A}_i, \mathbf{B}_i, \mathbf{C}_i)$ to denote the R1CS relation for the predicate that checks if the outcome of applying I_i on some input $(\overrightarrow{\mathsf{st}}, \overrightarrow{\mathsf{ReadVal}})$ is $\overrightarrow{\mathsf{st}'}$ (which contains values $\overrightarrow{\mathsf{WriteAddr}}$, $\overrightarrow{\mathsf{WriteVal}}$ in the appropriate registers).

Commit-and-Prove ZK Proof System for $\mathcal{R}^{\mathsf{zkRAM}}$. Let π^{LCom} be a linearly homomorphic commitment scheme, π^{zkDisj} be the protocol from Section 6 for the set of R1CS relations $(\mathbf{A}_i, \mathbf{B}_i, \mathbf{C}_i)_{i\in[\ell]}$ and π^{Memory} be the protocol for checking memory consistency from Section 5. Dora works as follows:

- *Setup* $\pi^{\mathsf{zkRAM}}_{\mathsf{Setup}}$*:* Sen and Rec invoke $\pi^{\mathsf{LCom}}_{\mathsf{Setup}}$ to obtain pp, skey and rkey.
- *Prove* $\pi^{\mathsf{zkRAM}}_{\mathsf{Prove}}$*:* We divide the prover protocol into an initialization phase and an execution phase:

  1. *Initialization Phase:* Sen and Rec proceed as follows:

- Invoke $\pi^{\mathsf{LCom}}_{\mathsf{Commit}}$ on $\overrightarrow{\mathsf{st}_0}, \overrightarrow{M_0}$ to get $\left[\!\left[\overrightarrow{\mathsf{st}_0}\right]\!\right]$ and $\left[\!\left[\overrightarrow{M_0}\right]\!\right]$.
- Invoke $\pi^{\mathsf{Memory}}_{\mathsf{Init}}$ on $\left[\!\left[\overrightarrow{M_0}\right]\!\right]$ to initialize the memory.
- Run the Initialization Phase of $\pi^{\mathsf{ZKDisj}}_{\mathsf{Prove}}$.

2. *Execution Phase:* For each $j \in [t]$, Sen and Rec proceed as follows:
   - Invoke $\pi^{\mathsf{LCom}}_{\mathsf{Commit}}$ to compute commitments $\left[\!\left[\overrightarrow{\mathsf{st}_j}\right]\!\right]$, $[\![\mathsf{inst}_j]\!]$, $\left[\!\left[\overrightarrow{\mathsf{ReadVal}_j}\right]\!\right]$, $\left[\!\left[\overrightarrow{\mathsf{OldWriteVal}_j}\right]\!\right]$. We assume that $\left[\!\left[\overrightarrow{\mathsf{st}_j}\right]\!\right]$ is a concatenation of commitments to the program counter $[\![\overrightarrow{\mathsf{pc}_j}]\!]$ and values stored in the registers including $\left[\!\left[\overrightarrow{\mathsf{ReadAddr}_j}\right]\!\right]$, $\left[\!\left[\overrightarrow{\mathsf{WriteAddr}_j}\right]\!\right]$, $\left[\!\left[\overrightarrow{\mathsf{WriteVal}_j}\right]\!\right]$. Use $\left[\!\left[\overrightarrow{\mathsf{ReadVal}_j}\right]\!\right]$, $\left[\!\left[\overrightarrow{\mathsf{st}_{j-1}}\right]\!\right]$, $\left[\!\left[\overrightarrow{\mathsf{st}_j}\right]\!\right]$ and invoke $\pi^{\mathsf{LCom}}_{\mathsf{Commit}}$ as needed to compute a commitment to the extended witness $[\![\overrightarrow{\mathsf{z}_{\mathsf{inst}_j}}]\!]$ for the relation $(\mathbf{A}_{\mathsf{inst}_j}, \mathbf{B}_{\mathsf{inst}_j}, \mathbf{C}_{\mathsf{inst}_j})$
   - Invoke $\pi^{\mathsf{Memory}}_{\mathsf{Read}}$ to read $[\![\mathsf{inst}_j]\!]$ from address $[\![\overrightarrow{\mathsf{pc}_{j-1}}]\!]$ and to read $\left[\!\left[\overrightarrow{\mathsf{ReadVal}_j}\right]\!\right]$ from address $\left[\!\left[\overrightarrow{\mathsf{ReadAddr}_j}\right]\!\right]$.
   - Invoke $\pi^{\mathsf{Memory}}_{\mathsf{Update}}$ to replace $\left[\!\left[\overrightarrow{\mathsf{OldWriteVal}_j}\right]\!\right]$ with $\left[\!\left[\overrightarrow{\mathsf{WriteVal}_j}\right]\!\right]$ at the location $\left[\!\left[\overrightarrow{\mathsf{WriteAddr}_j}\right]\!\right]$.
   - Finally, run the j^{th} step in the execution phase in $\pi^{\mathsf{ZKDisj}}_{\mathsf{Prove}}$ using $[\![\overrightarrow{\mathsf{z}_{\mathsf{inst}_j}}]\!]$ and branch index inst_j.

- *Verify* $\pi^{\mathsf{zkRAM}}_{\mathsf{Verify}}$*:* Sen and Rec invoke $\pi^{\mathsf{Memory}}_{\mathsf{Verify}}$, $\pi^{\mathsf{ZKDisj}}_{\mathsf{Verify}}$ and $\pi^{\mathsf{LCom}}_{\mathsf{Open}}$ on $[\![\mathsf{st}_t]\!]$ and $[\![M_t]\!]$. Output 1, if all these checks verify.

Theorem 7.1. *Assuming that π^{LCom} in a secure linearly homomorphic commitment scheme (see Section 3.1), π^{Memory} is a protocol for checking memory consistency (see Section 5) and π^{ZKDisj} be a commit-and-prove zero-knowledge for $\mathcal{R}^{\mathsf{ZKDisj}}$ as defined in Section 6. Then the above protocol $\pi^{\mathsf{zkRAM}} = (\pi^{\mathsf{zkRAM}}_{\mathsf{Setup}}, \pi^{\mathsf{zkRAM}}_{\mathsf{Prove}}, \pi^{\mathsf{zkRAM}}_{\mathsf{Verify}})$ is a LinCom-based commit-and-prove zero-knowledge as defined in Section 3.2 for $\mathcal{R}^{\mathsf{zkRAM}}$.*

Proof. **Correctness.** Correctness follows from correctness of Linearly Homomorphic commitment π^{LCom}, memory consistency protocol π^{Memory} and protocol for verifying processor execution π^{ZKDisj}.

Zero-Knowledge. Let $\mathsf{Sim}^{\mathsf{Memory}} = (\mathsf{Sim}^{\mathsf{Memory}}_{\mathsf{Setup}}, \mathsf{Sim}^{\mathsf{Memory}}_{\mathsf{Init}}, \mathsf{Sim}^{\mathsf{Memory}}_{\mathsf{Insert}}, \mathsf{Sim}^{\mathsf{Memory}}_{\mathsf{Remove}}, \mathsf{Sim}^{\mathsf{Memory}}_{\mathsf{VerEmpty}})$ be the simulator for π^{Memory} and let $\mathsf{Sim}^{\mathsf{ZKDisj}}$ be the simulator for π^{ZKDisj}. The simulator Sim for our π^{zkRAM} protocol proceeds like the Sen in an honest execution of π^{zkRAM}, except that: (1) Instead of running π^{Memory} honestly, it uses $\mathsf{Sim}^{\mathsf{Memory}}$ to simulate operations in π^{Memory}, (2) instead of running π^{ZKDisj} honestly, it uses $\mathsf{Sim}^{\mathsf{ZKDisj}}$ to simulate operations in π^{ZKDisj} and (3) whenever the parties invoke $\pi^{\mathsf{LCom}}_{\mathsf{Commit}}$ (except when committing to M_0), Sen computes a commitment to $\overrightarrow{0}$. Commitment to M_0 is computed honestly as described in the protocol.

We now show that view of the receiver when interacting with the simulator Sim is the computationally close to the view of the receiver interacting with the honest sender. We proceed with a hybrid argument. Let Hybrid_0 denote the interaction between the receiver and the honest sender.

- Hybrid_1 : Let Hybrid_1 be the same as Hybrid_0, but Sim simulates π^{Memory}. By the zero-knowledge property of π^{Memory}, the view of the receiver in Hybrid_1 and Hybrid_0 are computationally close.
- Hybrid_2 : This hybrid is similar to Hybrid_1, except that Sim simulates π^{ZKDisj}. By the zero-knowledge property of π^{ZKDisj}, the view of the receiver in Hybrid_1 and Hybrid_2 are computationally close.
- Hybrid_3 This hybrid is the same as Hybrid_2, except that instead of computing commitments to honestly computed (private) values, Sim computes commitments to $\overrightarrow{0}$. By the hiding property of π^{LCom}, view of receiver in Hybrid_2 and Hybrid_3 are computationally close.

Note that the view of the receiver in Hybrid_3 is distributed the same as the view of the receiver when interacting with the simulator above. Thus, we have concluded our proof.

Knowledge Soundness. Let $\mathcal{E}^{\mathsf{LCom}}$ be the extractor of the linearly homomorphic commitment scheme. Given a verifying proof transcript for π^{zkRAM}, the extractor $\mathcal{E}$ for our π^{zkRAM} protocol runs $\mathcal{E}^{\mathsf{LCom}}$ to simply extract the values from all commitments computed during the protocol. The probability that extracted values do not satisfy the relation $\mathcal{R}^{\mathsf{zkRAM}}$ as described in Section 7, depends on the following:

- $\mathcal{E}^{\mathsf{LCom}}$ failed to extract the correct value, which only happens with negligible probability due to the binding property of π^{LCom}.
- The adversary succeeds in violating knowledge soundness of π^{Memory}, which also happens with negligible probability.
- The adversary succeeds in violating knowledge soundness of π^{ZKDisj}, which also happens with negligible probability.

Therefore, the overall probability that this extractor fails to extract a satisfying set of extended witnesses from a verifying transcript is negligbly small. □

8 Implementation and Evaluation

In order to evaluate the concrete performance of Dora, we implement it and perform benchmarks. Specifically, we provide separate speed benchmarks for the memory consistency checks (Section 5) and processor instruction checks (Section 6). We find that this does a good job highlighting Dora's performance. Additionally, we find that our processor instruction check are the bottlenecks for performance (with each step taking several milliseconds), whereas memory consistency checks are virtually free in comparison (with each memory operation taking several microseconds). As such, the benchmarks for processor instructions are a sufficient estimate of Dora's end-to-end performance.

Implementation and Benchmark Configuration. We implement Dora in Rust on top of Galois' `swanky`[Gal19] framework, a suite of secure computation and zero-knowledge tools. Our code is intentionally designed to be interoperable with the emerging SIEVE intermediary representation (IR) [sie] standard such that it can interface with other emerging zero-knowledge techniques. Our code will be made public upon publication. To instantiate our linearly homomorphic commitments, we use vector oblivious linear evaluation (VOLE) base commitments, like other state-of-the-art interactive zero-knowledge protocols (e.g. QuickSilver [YSWW21]). `swanky` generates the prerequisite VOLE correlations using KOS OT-extension protocol[KOS15]. These correlations are computed "just-in-time," rather than in a pre-processing phase; the resulting interaction introduces a non-trivial overhead in our implementation which is included in all benchmarks. We also include all setup costs in our benchmarks. Our evaluation is done over a 61-bit prime field.

We run benchmarks on a typical, commodity laptop (`Intel i7-11800H @` 2.3 GHz and 64 GB of RAM). Additionally, we run benchmarks on an AWS server (`Intel Xeon Platinum 8259C`@ 2.50GHz and 128 GB of RAM); we include the benchmarks from this later configuration in Appendix A. We run the prover and verifier on the same hardware and simulate network conditions using `tc(8)` and `netem(8)`. The bandwidth in our benchmarks is limited to 1Gbps and we simulate multiple network latencies. Specifically, we simulate localhost/colocated computation (latency = 0ms), intracountry/intrastate settings (latency = 10ms) and Europe-to-West-Coast conditions (latency = 100ms).

8.1 Processor Instruction Checks

We begin by benchmarking our disjunctive zero-knowledge protocol that ensures each application of the processor circuit is done correctly (Section 6). We realize this protocol as a custom plugin for the SIEVE IR [sie] which takes in a set of functions (ie. the instructions) over which to do the disjunction. The result is a plugin that can be called with the same number of inputs and outputs as the provided functions.

In order to benchmark this construction, we generate uniformly random instruction circuits with a prescribed number of multiplication gates. We do this by repeatedly sampling a random addition/multiplication gate with probability $1/2$ until the desired number of multiplication gates is reached. To connect these gates, we sample random input wires for each new gate from the set of previous output wires. The result is circuits with random topology, a good approximation for the worst case for efficiency.

Network Latency: 0 ms

Mul. Per Clause	2^3	2^6	2^9	2^{12}	2^{15}
2^6	1138.10	1090.46	1166.00	1123.02	663.91
2^9	423.42	418.81	417.60	376.82	240.04
2^{12}	144.03	140.27	147.69	133.81	86.00
2^{15}	58.60	59.23	56.77	54.47	

Network Latency: 10 ms

Mul. Per Clause	2^3	2^6	2^9	2^{12}	2^{15}
2^6	1144.25	1156.57	1120.21	1126.51	650.81
2^9	417.90	435.79	412.70	374.88	240.71
2^{12}	150.02	148.25	145.24	131.49	82.76
2^{15}	60.03	58.46	58.07	53.08	

Network Latency: 100 ms

Mul. Per Clause	2^3	2^6	2^9	2^{12}	2^{15}
2^6	662.77	654.39	650.05	631.92	397.06
2^9	250.59	246.90	250.13	222.61	148.70
2^{12}	87.38	86.70	86.94	80.16	52.12
2^{15}	35.47	35.71	34.93	32.71	

Figure 5: ZK for disjunctions: number of disjunction applications per second. Running on `Intel i7-11800H`.

Benchmarks. We present the results of our benchmarks in two tables:

(1) In Figure 5, we show how many processor steps Dora proves per second for processors of varying complexity. To compute these values, we prove 50,000 copies of the processor circuit, where a random instruction is chosen in each step. We vary the number of multiplication gates in each instruction in the set $\{2^6, 2^9, 2^{12}, 2^{15}\}$ and vary the number of instructions supported by the processor in the set $\{2^6, 2^9, 2^{12}, 2^{15}\}$. Note that the overhead of setup and verifying the final R1CS instances grows as the number of instructions grows and the size of the instructions grows. When the number of instructions reaches 2^{15}, this overhead becomes non-trivial (compared to the fixed 50,000 steps) and begins to become visible in the benchmarks. We note that our machine ran out of memory for 2^{15} instructions of size 2^{15} simply because the overhead for holding the descriptions of the instructions was too high.

(2) In Figure 6, we aim to illustrate that the marginal cost of proving each additional step of the processor is constant in the number of instructions. To do this, we run the same experiment as in (1), but for 25,000 processor steps, interpolate between the two points and compute the time taken to prove each of the *additional* 25,000 steps. In this table, the asymptotic characteristic of Dora becomes very clear: the marginal cost per-step is constant as the number of instructions in the processor increases.

Recall that the total cost of proving a step of a processor in Dora is a single invocation of this protocol, plus several memory access operations. As we show in the next subsection, the costs of these memory operations are marginal compared to checking the processor instructions. As such, we use the benchmarks provided in Figure 5 and Figure 6 as a good approximation of the overall performance of Dora.

8.2 Memory Checking

We now turn our attention to benchmarking the memory consistency checking protocol presented in Section 5. When implementing this protocol, we integrate several minor changes. Namely, because of the high number of rounds in the ZKbag protocol we apply Fiat-Shamir to compute tag challenges, but we do not use Fiat-Shamir in the final consistency check. The resulting protocol remains designated verifier, as we still use VOLE for all commitments. Additionally, because the security of ZKBag is statistical in the size of the field (a 61-bit prime field), we need to

Network Latency: 0 ms

Mul. Per Clause	2^3	2^6	2^9	2^{12}	2^{15}
2^6	0.60 ms	0.69 ms	0.59 ms	0.63 ms	0.59 ms
2^9	2.36 ms	2.46 ms	2.37 ms	2.29 ms	2.56 ms
2^{12}	6.85 ms	7.36 ms	6.44 ms	6.58 ms	6.96 ms
2^{15}	16.97 ms	16.52 ms	18.07 ms	16.68 ms	

Network Latency: 10 ms

Mul. Per Clause	2^3	2^6	2^9	2^{12}	2^{15}
2^6	0.61 ms	0.56 ms	0.63 ms	0.62 ms	0.69 ms
2^9	2.42 ms	2.31 ms	2.52 ms	2.31 ms	2.61 ms
2^{12}	6.42 ms	6.52 ms	6.58 ms	6.70 ms	7.42 ms
2^{15}	17.02 ms	17.38 ms	17.01 ms	17.74 ms	

Network Latency: 100 ms

Mul. Per Clause	2^3	2^6	2^9	2^{12}	2^{15}
2^6	1.19 ms	1.24 ms	1.25 ms	1.17 ms	1.17 ms
2^9	3.94 ms	4.01 ms	3.92 ms	4.04 ms	3.98 ms
2^{12}	11.16 ms	11.35 ms	11.12 ms	11.21 ms	10.77 ms
2^{15}	28.36 ms	27.89 ms	27.73 ms	27.73 ms	

Figure 6: ZK for disjunctions: marginal cost for additional disjunction applications. Running on `Intel i7-11800H`.

$t = 2^{23}$	2^{12}	2^{14}	2^{16}	2^{18}	2^{20}
0 ms	545387	545352	545210	547773	543268
10 ms	501591	513535	508092	517432	514070
100 ms	202618	204475	206942	200344	192602

Figure 7: Number of RAM operations (READ/WRITE) per second. Running on `Intel i7-11800H`.

sample two field elements for each tag. With this approach we get ≈ 122 bits of computation security. The rest of the protocol is unmodified.

Benchmarks. As before, present the results of our benchmarks in two tables:

(1) In Figure 7 we show the average number of memory operations (READ/WRITE) per second averaged over 2^{23} operations. To illustrate that the size of the memory does not meaningfully impact performance, we initialize a memory space of size $\{2^{12}, 2^{14}, 2^{16}, 2^{18}, 2^{20}\}$.

(2) In Figure 8 we show the marginal cost of each additional memory operation to highlight the asymptotic behavior of our construction. We do this by computing the difference in runtime for performing 2^{22} operations and 2^{23} operations.

We note that performance starts to degrade when the network latency hits 100ms. This is an artifact of the on-demand nature of the VOLE computation in `swanky`. Because correlations are not computed upfront, the computation must pause in order to generate more VOLE correlations. Because this correlation generation protocol is a multi-round protocol, when the latency increases VOLE correlation generation dominates the overall cost. We emphasize that this is not a fundamental limitation of the protocol but rather a limitation of `swanky`. By using Fiat-Shamir, the online phase of our protocol becomes constant round and the required number of correlations could be computed in an offline phase.

$t \in \{2^{22}, 2^{23}\}$	2^{12}	2^{14}	2^{16}	2^{18}	2^{20}
0 ms	$1.63\mu s$	$1.62\mu s$	$1.62\mu s$	$1.62\mu s$	$1.60\mu s$
10 ms	$1.91\mu s$	$1.77\mu s$	$1.86\mu s$	$1.77\mu s$	$1.68\mu s$
100 ms	$4.53\mu s$	$4.49\mu s$	$4.38\mu s$	$4.48\mu s$	$4.31\mu s$

Figure 8: Observe that the marginal cost for a RAM access is independent of the size of the memory space. Running on `Intel i7-11800H`.

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A Comparison with Concurrent Work

The concurrent works of Yang et al. [YHH+23] [CCS 2023] and Yang and Heath [YH23] [USENIX Security 2024] are both deeply related to the RAM zero-knowledge approach we develop in this work. More specifically, Yang et al. [YHH+23] proposed Batchman and Robin, a pair of techniques that produce interactive zero-knowledge specially designed for proving a batch of disjunctions (eg. a set of processor circuits). Yang and Heath [YH23] proposed a new approach for creating zero-knowledge random access memory based on a pair of permutation proofs.

Although not done, it is straight forward to combine these two works to achieve a RAM zero-knowledge protocol with better/similar concrete performance as Dora for a small/moderate number of instructions, although the asymptotic behavior of Dora is better. We believe that our work is complementary to these results, as we provide a different set of techniques that reach the same overarching goal. Additional research is required to identify the best way to combine these techniques in order to produce performant zero-knowledge proofs of RAM program execution in many settings and it is likely that viewing these three works together will uncover new techniques.

Given the concurrent nature of the works, we give a best-effort comparison with Dora below. In general, we find that the microbenchmarks in Dora are slightly slower than the respective performance metrics reported in [YHH+23] and [YH23]. We note, however, that the comparison reduces to concrete constants, and thus even minor engineering choices could influence this comparison.

Batchman and Robin [YHH+23]. Yang et al. [YHH+23] begin by proposing Robin, a more communication efficient approach to disjunctive, VOLE-based zero-knowledge. Their key insight is that the prover and verifier, given a linearly homomorphic commitment to an extended witness, can compress that satisfiability check of each clause in the disjunction down to a constant size check (ie. if a committed value is 0). This protocol requires only a single random challenge from the verifier. They then propose Batchman, a way to *batch* many instances of these disjunctive statements together. They accomplish this by having the prover commit to the branch they want to satisfy in each statement in the batch, and then do a bespoke membership proof to show that the commitment contains a valid clause.

We note that Batchman does a small linear amount of work in the number of clauses in the disjunction, meaning Dora's asymptotic behavior is slightly better. However, we believe that using a ZKBag (or the read-only memory construction from [YH23]), the scheme can be improved to avoid this linear dependence on the number of clauses.

We provide benchmarks for proving disjunctions with Dora on equivalent hardware used to evaluate Batchman in Figure 10. Additionally, we prove a marginal, per-step timing on this hardware in Figure 11. In order to attempt to provide apples-to-apples comparisons of our evaluations, we contacted the authors of [YHH+23] to obtain results for a greater number of clauses (see Figure 9) on a machine similar to the server (`Intel Xeon Platinum 8259C`) we used for our benchmarks. Although their setup is slightly different (e.g. consisting of two independent colocated machines), we observe that for the same bandwidth (1 Gbps) and 2^{15} clauses Dora has very similar performance (see Figure 10).

Two Shuffles Make a RAM [YH23]. Yang and Heath also recently proposed a new approach for creating zero-knowledge random access memory. Their approach, which is very similar to ours, uses two permutation proofs to ensure that memory is treated consistently. While Dora uses time-stamping to ensure that a prover does not "read from the future," Yang and Heath use set membership proofs (which they implement using one of their permutation proofs). Their approach yields a *circuit* for random access memory, while ours results in a *protocol*. We provide benchmarks to compare concrete performance of our schemes, but note that the two share are conceptual core such that we would not anticipate performance to significantly diverge.

We provide benchmarks for memory access with Dora on equivalent hardware used in [YH23] in Figure 12 and marginal, per-access timing on this hardware in Figure 13. In Figure 10 of [YH23], the authors report $\sim 1.5\mu s$ per memory operation, while Dora's performance is $\sim 3\mu s$.

Gates Per Clause 2^{15}	1 Gbps	500 Mbps	100 Mbps	50 Mbps
2^9	148.62	109.99	36.09	19.42
2^{12}	82.88	63.09	21.77	11.84
2^{15}	17.88	14.08	5.16	2.89

Figure 9: Batchman performance. Showing the number of disjunction applications per second for 2^{15} clauses with varying numbers of multiplication gates.

Network Latency: 0 ms

Mul. Per Clause	2^3	2^6	2^9	2^{12}	2^{15}
2^6	657.89	657.92	653.18	648.31	479.91
2^9	246.06	246.49	245.81	242.40	179.95
2^{12}	87.37	86.47	85.99	81.70	62.20
2^{15}	35.14	34.85	34.38	32.92	

Network Latency: 10 ms

Mul. Per Clause	2^3	2^6	2^9	2^{12}	2^{15}
2^6	650.10	654.53	650.02	637.90	474.17
2^9	245.26	245.45	243.59	242.27	179.52
2^{12}	86.56	86.26	85.70	81.95	61.89
2^{15}	35.17	34.66	34.43	32.91	

Network Latency: 100 ms

Mul. Per Clause	2^3	2^6	2^9	2^{12}	2^{15}
2^6	474.38	472.92	473.04	464.44	349.20
2^9	177.09	178.46	177.06	174.42	131.27
2^{12}	62.89	62.93	62.64	59.91	45.69
2^{15}	25.36	25.36	25.15	24.15	

Figure 10: ZK for disjunctions: number of disjunction applications per second. Single-threaded running on `Intel Xeon Platinum 8259C`. See Section 8 for details on the experimental setup.

Network Latency: 0 ms

Mul. Per Clause	2^3	2^6	2^9	2^{12}	2^{15}
2^6	1.50 ms	1.50 ms	1.52 ms	1.52 ms	1.52 ms
2^9	4.06 ms	4.00 ms	4.00 ms	3.63 ms	4.14 ms
2^{12}	11.19 ms	11.38 ms	11.41 ms	11.48 ms	11.71 ms
2^{15}	28.22 ms	28.46 ms	28.71 ms	29.21 ms	

Network Latency: 10 ms

Mul. Per Clause	2^3	2^6	2^9	2^{12}	2^{15}
2^6	1.53 ms	1.51 ms	1.52 ms	1.56 ms	1.55 ms
2^9	4.05 ms	4.08 ms	4.06 ms	3.55 ms	4.08 ms
2^{12}	11.34 ms	11.29 ms	11.34 ms	11.38 ms	11.86 ms
2^{15}	28.02 ms	28.59 ms	28.34 ms	28.92 ms	

Network Latency: 100 ms

Mul. Per Clause	2^3	2^6	2^9	2^{12}	2^{15}
2^6	2.04 ms	2.08 ms	2.08 ms	2.10 ms	2.11 ms
2^9	5.65 ms	5.55 ms	5.57 ms	5.13 ms	5.65 ms
2^{12}	15.57 ms	15.51 ms	15.63 ms	15.60 ms	16.16 ms
2^{15}	39.11 ms	39.30 ms	39.22 ms	39.87 ms	

Figure 11: ZK for disjunctions: marginal cost (time) for any additional disjunction applications. Single-threaded running on `Intel Xeon Platinum 8259C`. See Section 8 for details on the experimental setup.

$t = 2^{23}$	2^{12}	2^{14}	2^{16}	2^{18}	2^{20}
0 ms	304619	304486	304089	303528	300505
10 ms	294554	294709	294771	293246	290424
100 ms	167889	167567	166947	164563	158010

Figure 12: ZK for memory operations: number of RAM operations (READ/WRITE) per second. Running on `Intel Xeon Platinum 8259C`. See Section 8 for details on the experimental setup.

$t \in \{2^{22}, 2^{23}\}$	2^{12}	2^{14}	2^{16}	2^{18}	2^{20}
0 ms	$2.89\mu s$	$2.90\mu s$	$2.89\mu s$	$2.89\mu s$	$2.88\mu s$
10 ms	$2.98\mu s$	$2.97\mu s$	$2.99\mu s$	$2.99\mu s$	$2.99\mu s$
100 ms	$5.31\mu s$	$5.32\mu s$	$5.29\mu s$	$5.36\mu s$	$5.26\mu s$

Figure 13: ZK for memory operations: marginal cost (time) for any additional RAM operations (READ/WRITE). Running on `Intel Xeon Platinum 8259C`. See Section 8 for details on the experimental setup.